TABLE OF CONTENTS

TABLE OF ILLUSTRATIONS

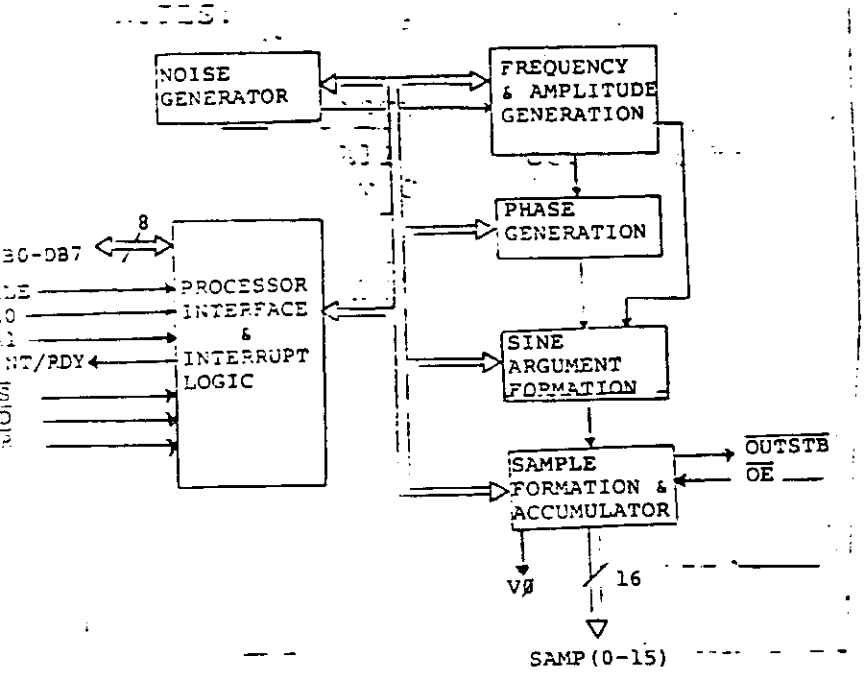
1. GENERAL DESCRIPTION

AMY1 is a digital, pipeline architectured, additive music synthesizer chip. There are 8 voices maximum assignable with a total of 64 harmonic oscillators, available in groups of two, for voice assignment. AMY1 has 72 independent, piecewise linear envelope generators: 8 fundamental frequency envelopes and 64 harmonic amplitude envelopes. A complete sound system requires addition of a D/A converter IC (up to 16 bit). To provide higher level commands, the system will generally include a controlling processor such as the Intel 8051 single chip microcomputer.

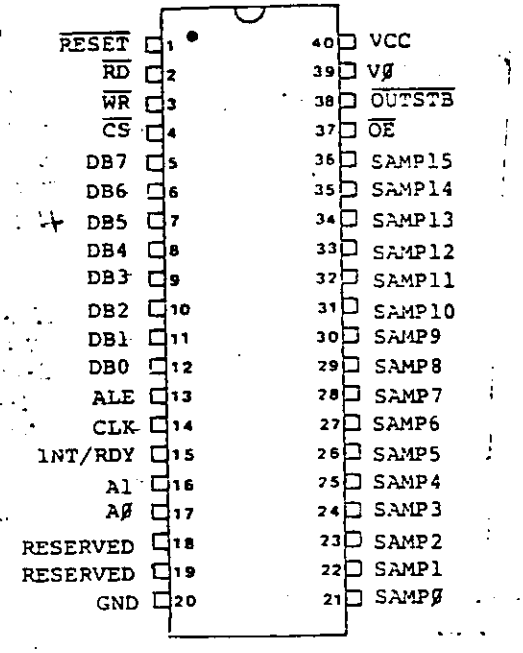
2. FEATURES

- o Single 40 pin DIP
- o 3u NMOS technology
- o Pipeline architecture
- o 5 MHz external clock frequency (maximum)
- o Integrated exponential ROM
- o 1/128 dB harmonic amplitude resolution & 1/64 semitone fundamental frequency resolution
- o $\overline{\text{Interrupt}}$/Ready pin
- o Bus compatible with multiplexed and non-multiplexed bus microprocessors
- o Full 16 bit digital output width
- o Independent voice mode
- o Adjustable sample rate
- o Programmable noise statistics
- o 72 on chip envelope generators
- o Approximately 37,000 transistors

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

Pin Name	Type	Pin #	Function
Vcc	I	40	+5 volt supply (±10%).
GND	I	20	Ground.
$\overline{\text{RESET}}$	I	1	Reset. When low, performs a master reset on the AMY 1 chip. This signal asynchronously terminates device activity and clears the System Options register, System Control register, Sequencer, Control Counter, Subsample Counter, Phase RAM and Digital Output Word (SAMP bus).
A1-A0	I	16-17	Address lines. Used to select internal AMY 1 registers when not in ALE mode. A1 is the most significant bit. A1 and A0 should be tied to Ground when ALE mode is used.
$\overline{\text{RD}}$	I	2	Read strobe. Used to transfer contents of selected register onto the data bus line (DB0-DB7). CS pin must be low to enable the AMY bus drivers.
$\overline{\text{WR}}$	I	3	Write strobe. Used to load the selected AMY register from the data bus lines (DB0-DB7). CS must be low for the transfer to take place.
$\overline{\text{CS}}$	I	4	Chip select. When low, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins are enabled. When high, DB7-DB0 are tri-stated. The only time that AMY drives the data bus (DB7-DB0) is when CS = RD = 0.
CLK	I	14	3 to 5 MHz external clock.
DB7-DB0	I/O	5-12	8 bit, tri-state data bus used to transfer data and commands between AMY1 and the controlling CPU. DB7 is the most significant bit.
SAMP15-SAMP0	O	36-21	16 bit data bus used to transfer data from AMY to an external D/A converter. ~~DB15~~ SAMP15 is the most significant bit. This bus is tri-stated unless the $\overline{\text{OE}}$ pin is low. This allows more than one device to share a single D/A converter.
$\overline{\text{OUTSTB}}$	O	38	Output strobe. When low, indicates that valid data is on the SAMP bus. See Output Timing diagram (Section 12.2).

5. PIN DESCRIPTION (continued)

Pin Name	Type	Pin #	Function
INT/RDY	I	15	Interrupt/Ready. When operating in the READY mode, this pin is high only when AMY is not executing a command. In the INTERRUPT mode, the pin generates a 1 clock period wide pulse when completing a command.
ALE	I	13	Address latch enable. When enabled, latches address information from the DB0 and DB1 bits of the data bus. The A0 and A1 pins are grounded when this pin is used. When not in use, ALE should be grounded.
V0	O	39	Voice zero. When operating in the INDIVIDUAL mode, the V0 pin will be high during one OUTSTB pulse per sample period. During this particular OUTSTB the data on the SAMP bus is the current sample for Voice 0.
$\overline{OE}$	I	37	Output enable. When low, the output SAMP ~~DB~~ data bus is enabled. When high, the output ~~DB~~ SAMP data bus is disabled.
RESERVED	-	18,19	Undefined.

6. FUNCTIONAL DESCRIPTION

6.1 Musical Specifications

Given a CLK frequency of 4 MHz with 64 Harmonics enabled:

Amplitude Dynamic Range	63.75 dB
Minimum Amplitude Slope	1.91 dB/sec
Maximum Amplitude Slope	3784 dB/sec
Fundamental Frequency Range	$\hat{=}$ 4.8 Hz to 7.8 KHz (10 2/3 octave range)
Minimum Fundamental Frequency Slope	5.97 cents* /sec
Maximum Fundamental Frequency Slope	118 semitones/sec = 9.85 octaves/sec
Maximum Amplitude Increment	31/128 = 0.242 dB
Maximum Fundamental Frequency Increment	31/2048 = 1.51 cents
Number of Harmonics	64 (maximum)
Number of Voices	8 (maximum)
Number of Harmonics/Voice	Any multiple of 2
Harmonic Distortion	< 1%

* 1 cent = 1/100 of a semitone

4.2 Internal Architecture

AMY1 consists of 8 major blocks as shown in Figure 1 below.

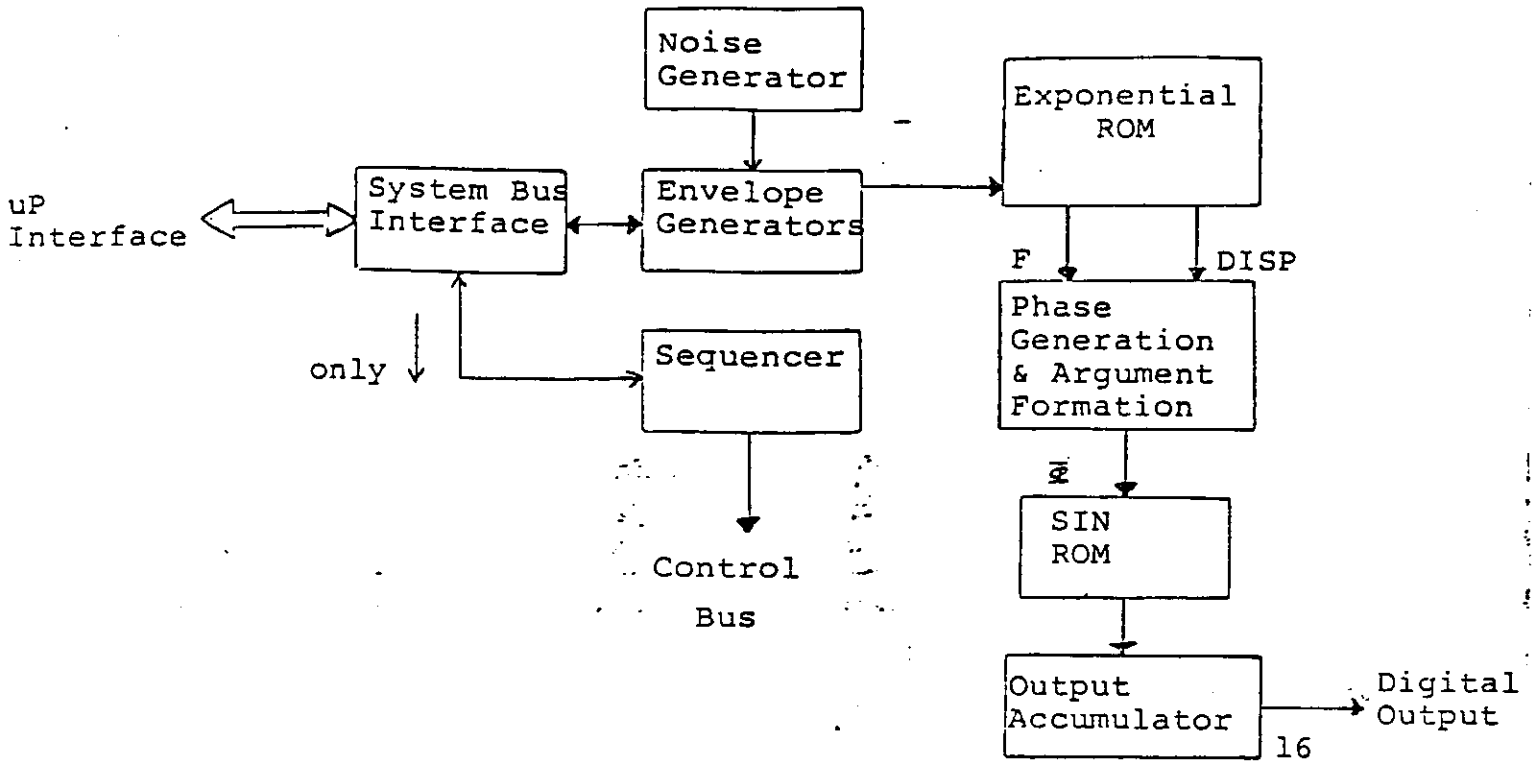


Figure 1. Simplified Block Diagram

The System Bus Interface block provides the user with a standard microprocessor interface. The user sends all commands and passes frequency and amplitude breakpoint data and current values over the "uP Interface" lines (RESET, RD, WR, CS, DB(0-7), ALE, INT/RDY, A1, A0).

The Noise Generator block contains a small RAM, a serial adder, and some associated logic. It generates two different channels of bandlimited white noise simultaneously. Bandwidths are programmable by initialization of the Noise RAM.

Internal Architecture (continued)

The Envelope Generator block contains the Voice RAM (VRAM), the Harmonic RAM (HRAM) and logic necessary to generate the 72 piecewise linear envelopes (8 fundamental frequency envelopes and 64 harmonic amplitude envelopes). The RAMs maintain a slope value, destination value and current value for each of the 72 envelopes (see Figure 2). The Voice RAM, in addition to slope, destination and current value, contains a 2 bit field for voice type selection. The total Envelope Generator RAM size is (64 * 29) + (21 * 16) bits = 278 bytes.

HRAM Data Word Format

13	8	8
Harmonic Amplitude Current Value	Harmonic Amplitude Destination	Harmonic Amplitude Slope

VRAM Data Word Format

13	8
Fundamental Frequency Destination	Fundamental Frequency Slope

and

18	2	1
Fundamental Frequency Current Value	Voice Type Select	Spare

Figure 2. HRAM and VRAM Data Word Format

The Envelope Generator block also contains the Last Harmonic Pair Flags (32) and an assortment of adders and other logic to generate all AMY envelopes from breakpoint information placed in the HRAM and VRAM by the sequencer under direction of the System Bus Interface command decoder. The Envelope Generator block also contains a Noise Adder. This is used in generating noise based voices.

The Exponential ROM converts the outputs of the 72 envelope generators to a piecewise exponential form for use internally. The ROM permits the AMY user to use decibel units for harmonic amplitude specification and semitone units for fundamental frequency specification. Not only are data widths reduced between the user and AMY, but master amplitude scaling and transposition operations are reduced to simple addition operations in the controlling processor.

The Sequencer block controls all the other blocks. It contains a 7 bit clock period counter and 7 bit subsample counter.

6.3 Complete AMY System

A complete sound system requires the addition of a D/A converter chip (up to 16 bit). To provide higher level commands the system will generally include a controlling such as the Intel 8051 Single Chip Microcomputer (see Figure 3 below).

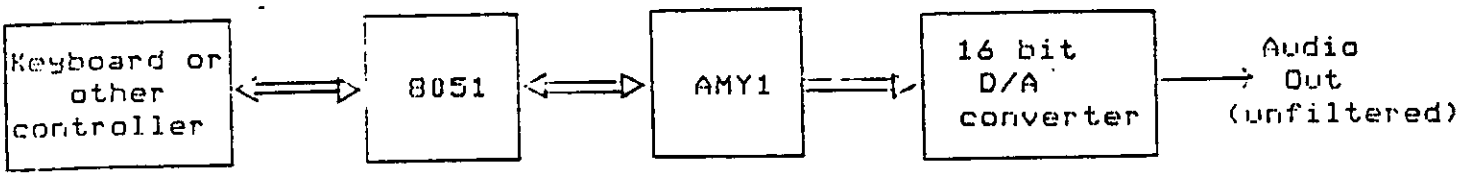


Figure 3. Complete AMY System Block

4.4 Envelope Generation

Envelopes are generated by the on chip AMY envelope generator block. The user may command the generators to make any piecewise linear envelope desired by using a slope and destination scheme. Assume that a particular envelope generator has been previously loaded immediate to zero. By loading two breakpoints (slope-destination pairs) we can generate the following envelope:

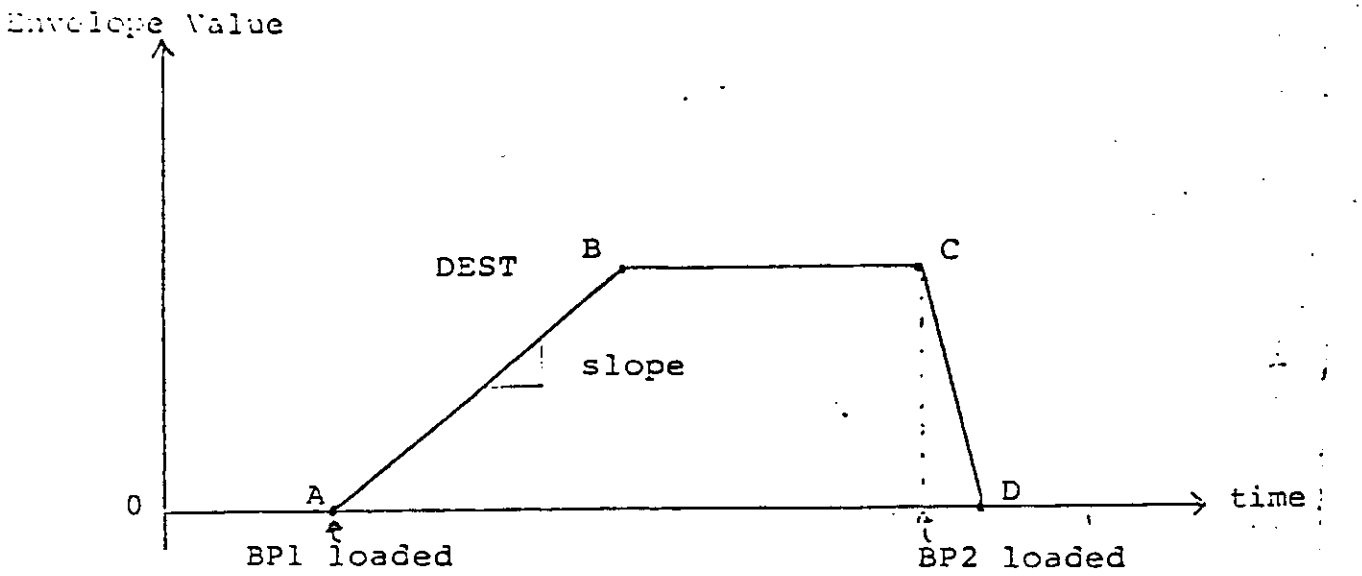


Figure 4. Piecewise linear envelope.

At point A, BP1 is loaded and the envelope starts rising at a constant slope determined by the "slope" value of BP1. The envelope generator will continue to increase in value until the DEST value is reached. Point B is called a "Free point" since a change in slope has occurred without the user having to load another BP. At Point C, a BP with negative slope and a DEST of zero has been loaded into AMY. The absolute value of the slope in BP2 is larger than that of BP1 , and thus it takes less time for the envelope to "fall" than it did to "rise." Point D is another free point since when the DEST of zero is reached the envelope remains a zero (slope is effectively cleared when the destination is reached).

Obviously, to achieve "smooth" pitch and amplitude modulation the "step" must be small. AMY supports a pitch step of 1/2048 of a semitone (≙ 0.0028% change in frequency) or in music terms 0.0488 cents. The amplitude step is 1/128 of a decibel. Both the pitch and amplitude steps were chosen so that pitch and amplitude envelopes will be sensed as "continuous" to the human ear for all AMY slope values:

Maximum Amplitude Increment = ± 31/128 dB,
Maximum Fundamental Frequency = ± 31/2048 semitones

The harmonic envelope generators have a dynamic range of 64 dB, therefore the <u>total amplitude slope dynamic range</u> is:

$1984 * 10^{64\ dB/20} \triangleq 3.2 \times 10^6$ to 1 (In volts/sec)

The pitch (fundamental frequency) has a range of 10 2/3 octaves or 128 semitones. This implies a <u>frequency slope dynamic range</u> of:

$1984 * 2^{10.667} \triangleq 3.2 \times 10^6$ to 1 (in Hz/sec)

6.4.1 Slope format

It is desirable to have a very wide range of slopes from nearly instantaneous changes in amplitude or pitch to nearly unperceivable changes in amplitude or pitch. To provide the AMY user with an adequate range of slopes, an exponential format is used for all AMY slopes. With this format, and also because all envelopes are exponentiated by the exponential ROM before use in the "oscillator" section of AMY, a tremendous dynamic range is accomplished (see Section 6.1, Musical Specification). The AMY slope format is:

sign bit	exponent	2's complement signed mantissa
7	6 5	4 3 2 1 0

Each AMY Harmonic Envelope Generator and Fundamental Frequency (pitch) Envelope Generator has its own slope byte. The sign bit determines whether the slope shall be positive or negative. The mantissa absolute value may range from 1 to 31 (or be 0). The exponent determines how often the mantissa is added (2's complement) to the current value of a particular envelope. If the exponent bits are both one (11), the envelope will be stepwise increased or decreased every other sample period. An exponent of "10" reduces the rate by a factor of 4 to every 8th sample period. An exponent of "01" reduces the rate by another factor of 4 to every 32nd sample period. Finally, an exponent of "00" causes its corresponding envelope to be integrated only every 128 sample periods. Table 1 shows relative slopes for some sample slope bytes.

Slope Byte								Relative Slope (steps/sample)
+/-	E1	E0	M4	M3	M2	M1	M0	
0	0	0	0	0	0	0	1	+1 step/128 sample periods = 7.8×10^{-3}
1	0	0	1	1	1	1	1	-1 step/128 sample periods = 7.8×10^{-3}
0	0	1	0	0	0	1	1	+3 steps/32 sample periods = 0.094
0	1	1	1	1	1	1	1	+31 steps/2 sample periods = 15.5
1	1	0	0	0	1	0	0	-28 steps/8 sample periods = -3.5
1	1	1	0	0	0	0	1	-31 steps/2 sample periods = -15.5

Table 1. Slope Examples

Notice that the ratio of the maximum to minimum slope is $15.5/7.8 \times 10^{-3}$

6.4.2 Destination Format

Since all harmonic amplitudes have a 64 dB dynamic range, a single 8 bit byte is used as a destination value for each harmonic amplitude. This leads to an amplitude destination resolution of:

$$\frac{64 \text{ dB}}{256} = 1/4 \text{ dB}$$

Harmonic Amplitude Destination Format and Examples

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Zero Amplitude
1	1	1	1	1	1	1	1	Full Scale (63.75 dB)
0	0	0	0	0	0	0	1	Minimum Harmonic Amplitude (0.25 dB)

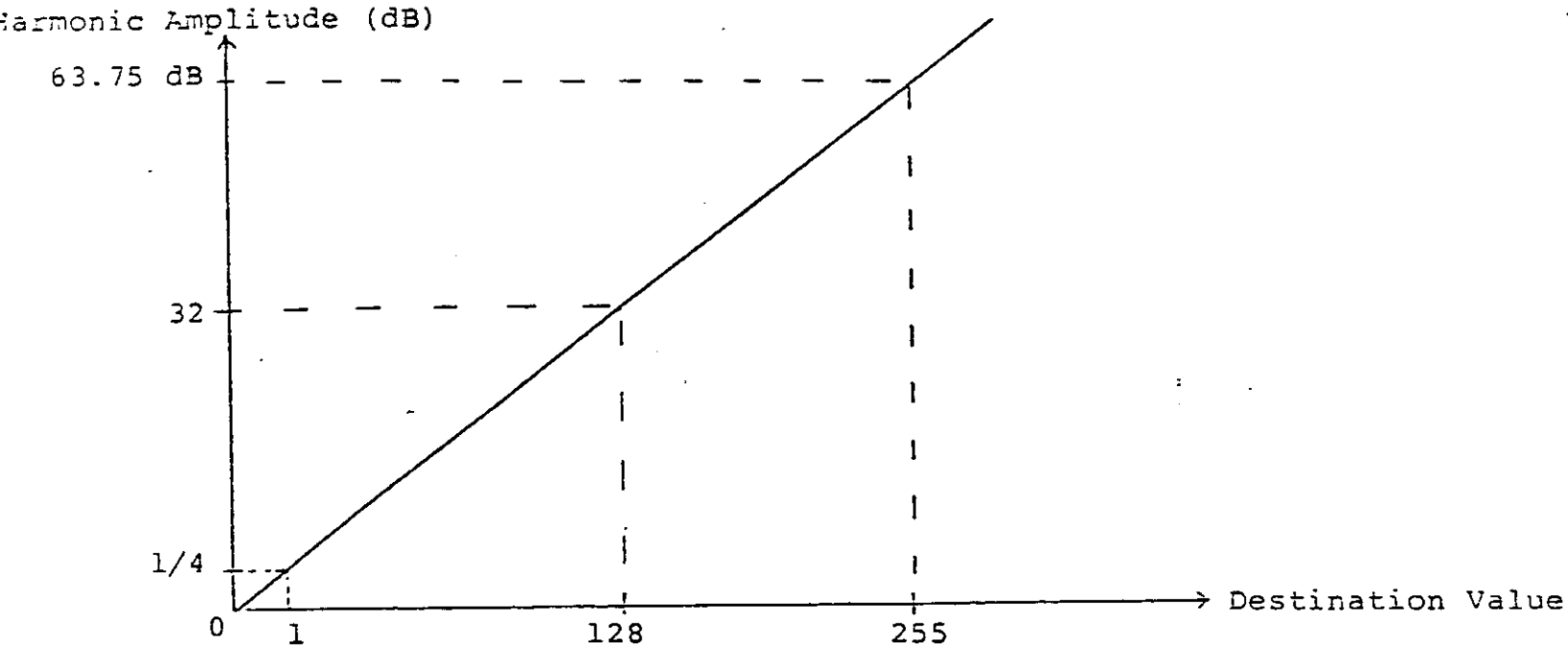
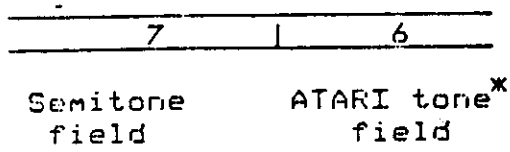


Figure 5. Linear Function of Harmonic Amplitude Destination

Destination Format (continued)

Since all Fundamental Frequency envelope generators have a 128 semitone range and a frequency resolution of 1/64 semitones for the Destination is desirable, 13 bits are used in the Frequency destination word.

Frequency Destination Format



Again the Fundamental Frequency (in semitones) is a linear function of Destination value.

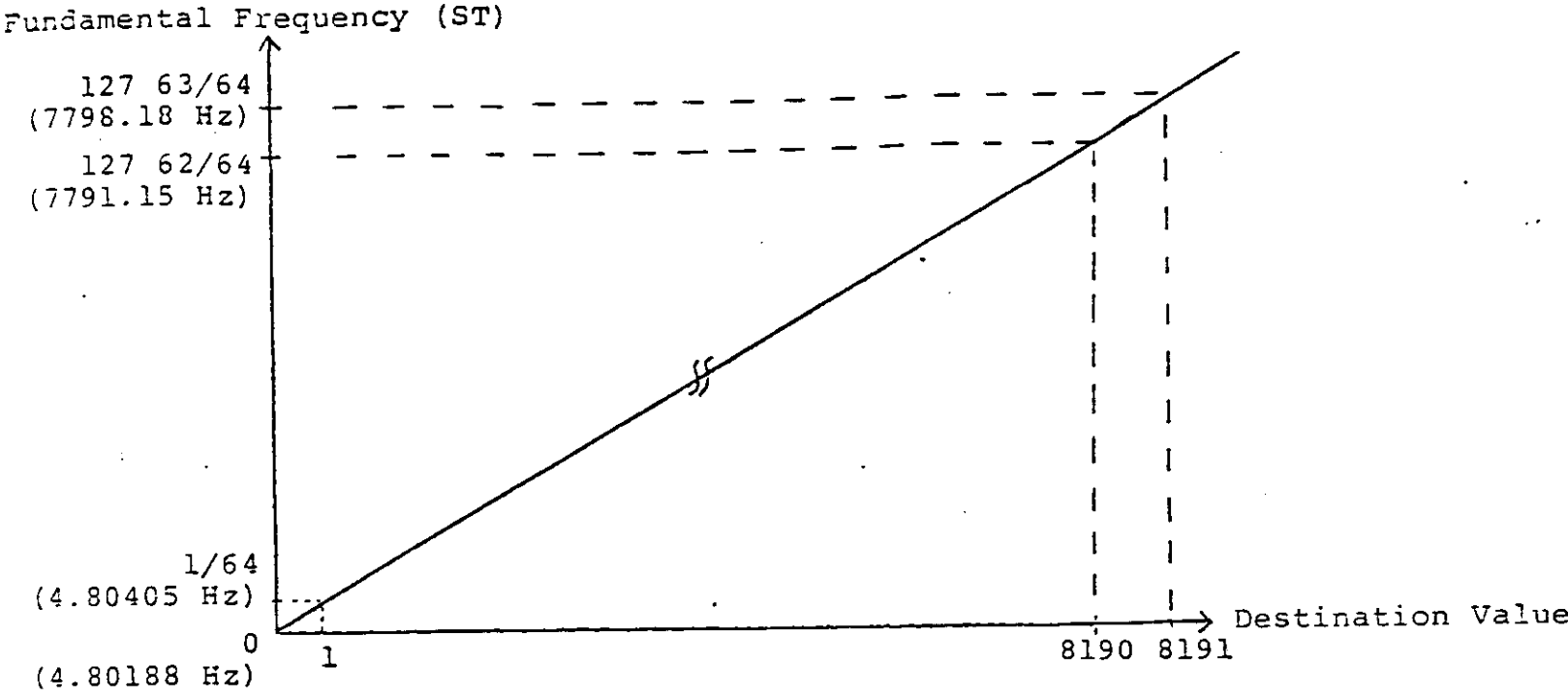


Figure 6. Fundamental Frequency vs. Destination

Notice that a Destination value of 0000 Hex yields a non-zero frequency and that the frequency resolution around 0 is ≙ 0.002 Hz per ATARI tone; at 8191 (or 1FFF Hex), the frequency resolution drops to ≙ 7 Hz per ATARI tone. This is desirable and is made possible by the exponential ROM.

Complete slope tables, computed for 4 MHz clock rate using 64 harmonics, are included in Appendix I.

*1 ATARI tone = 1/64 semitone

7. [illegible]

7.1 AMY Command Set

A command may be sent to AMY by setting $\overline{CS}$ = A1 = 0, $\overline{RD}$ = 1 and $\overline{WR}$ = 0. The command will be latched internally off the data bus on the trailing edge of the WR pulse. Each 8 bit command contains an opcode from 2 to 5 bits in length, and one or more operands (see Table 2 below).

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
0	0	0	0	1	V2	V1	V0	Write Fundamental Frequency Breakpoint
0	0	0	1	0	V2	V1	V0	Write Voice Type
0	0	0	1	1	V2	V1	V0	Read Current Fundamental Frequency
0	0	1	0	S03	S02	S01	S00	Write System Options.Register
0	0	1	1	X	X	SC1	SC0	Write System Control Register
0	1	H5	H4	H3	H2	H1	H0	Write Harmonic Amplitude Breakpoint
1	0	HP4	HP3	HP2	HP1	HP0	D0	Write Last Harmonic Pair Flag (Load SC1 bit = 0)
1	0	N5	N4	N3	N2	N1	N0	Write Noise RAM (Load SC1 bit = 1)
1	1	H5	H4	H3	H2	H1	H0	Read Current Harmonic Amplitude

Table 2. AMY Commands

V2-V0: Voice Number
S03-S00: System Options register bits
SC1-SC0: System Control register bits
H5-H0: Harmonic Number
HP4-HP0: Harmonic Pair Number
N5-N0: Noise RAM location
X: Don't care

7.2 RAM and Register Areas

User access to internal RAM and register areas is through 4 eight bit registers: 3 data (Reg A, Reg B, Reg C) and one command register. Figure 7 shows all AMY registers and RAM areas which are manipulated by the AMY command set. To write to AMY (e.g. "Write Fundamental Frequency Breakpoint" command), the user first sets up the proper values in the data registers A, B, and C, then issues the command to AMY's Command register.

When reading data from AMY (e.g. "Read Current Fundamental Frequency" command), the user first writes the command to the Command register, then reads the value from the data registers.

Each of the 4 registers is read (RD=0) or written (WR=0) to through the data bus lines DB0-DB7 using a unique address on A0-A1 (see Table 3). In the case of a read from the Command register, AMY's internal bus will appear on DB0-DB7. This has no operational use and is provided fro diagnostic purposes.

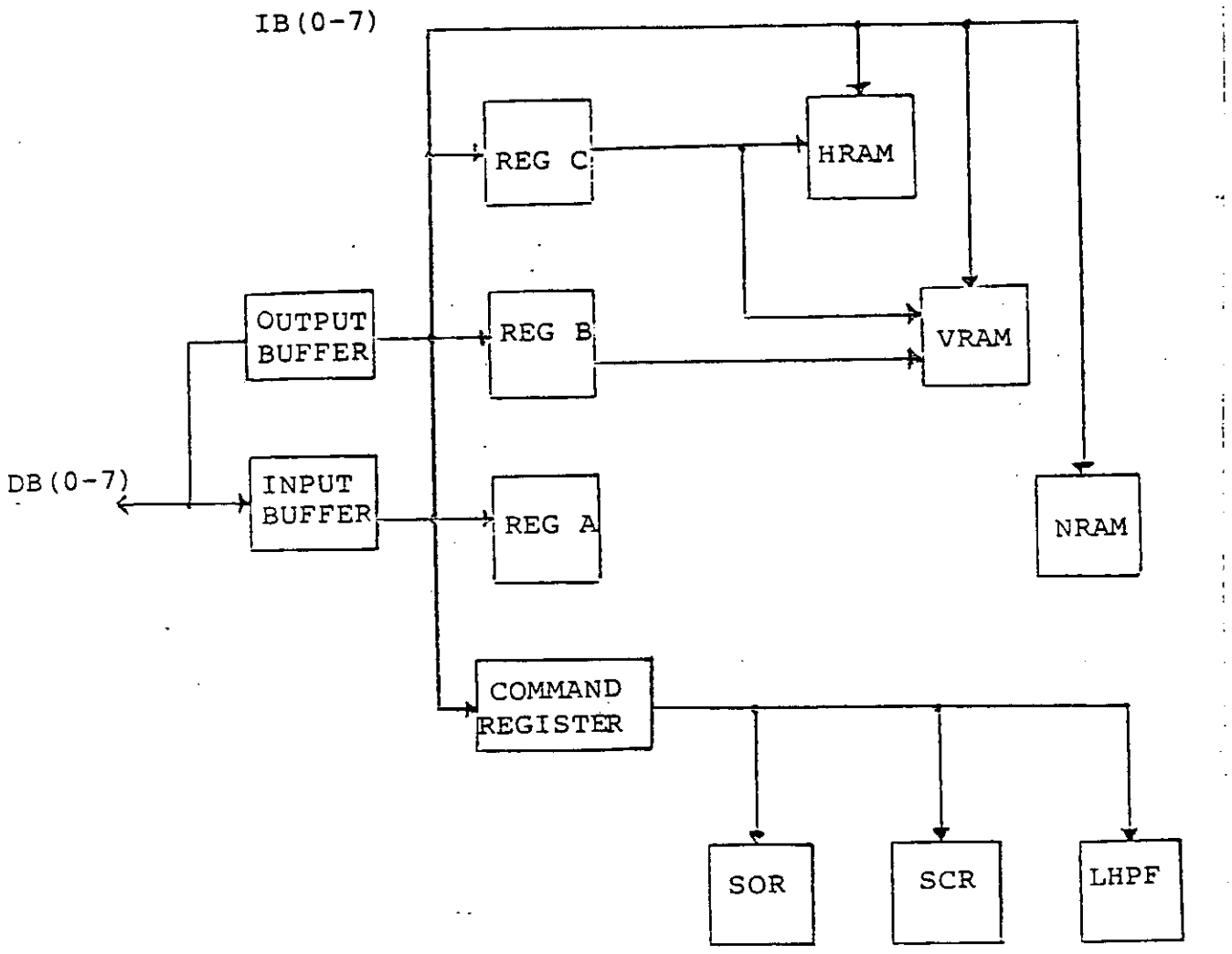


Figure 7. AMY RAM and Register Areas

7.3 AMY Data Registers

There are 3 data registers for passing data between the user and AMY internal RAM and Register storage areas. In general, the user loads the registers before sending a 'Write' command to AMY (e.g. "Write Fundamental Frequency Breakpoint"). Likewise, the user will read data from the registers after sending a 'Read' command to AMY (e.g. "Read Current Fundamental Frequency"). The registers are named Reg A, Reg B, and Reg C and are always directly accessible to the user since they have unique addresses (see Table 3).

$\overline{CS}$	A1	A0	Register Selected
0	0	0	Command (Write only)
0	0	1	Reg A
0	1	0	Reg B (Read or Write)
0	1	1	Reg C
1	X	X	None

Table 3. Register Selection

Data bus lines DB0 through DB7 are used to pass all data between the user and the AMY registers. DB0 through DB7 act as inputs (tri-state) unless RD = CS = 0, in which case the bus is driven by AMY with the contents of the selected register. If the Command register is selected, the AMY internal bus will be read.

8. OPERATING PROCEDURE

8.1 Initialization

8.1.1 RESET pin and Power up Sequence

Two milliseconds after power up, when spec power supply and clock requirements are met by the AMY interface circuit, the RESET pin may be released (see Figure 8). Alternatively, 2 ms after power up (and before), the RESET pin must be held equal to or less than the V_{IL} spec for the RESET pin (see Figure 9).

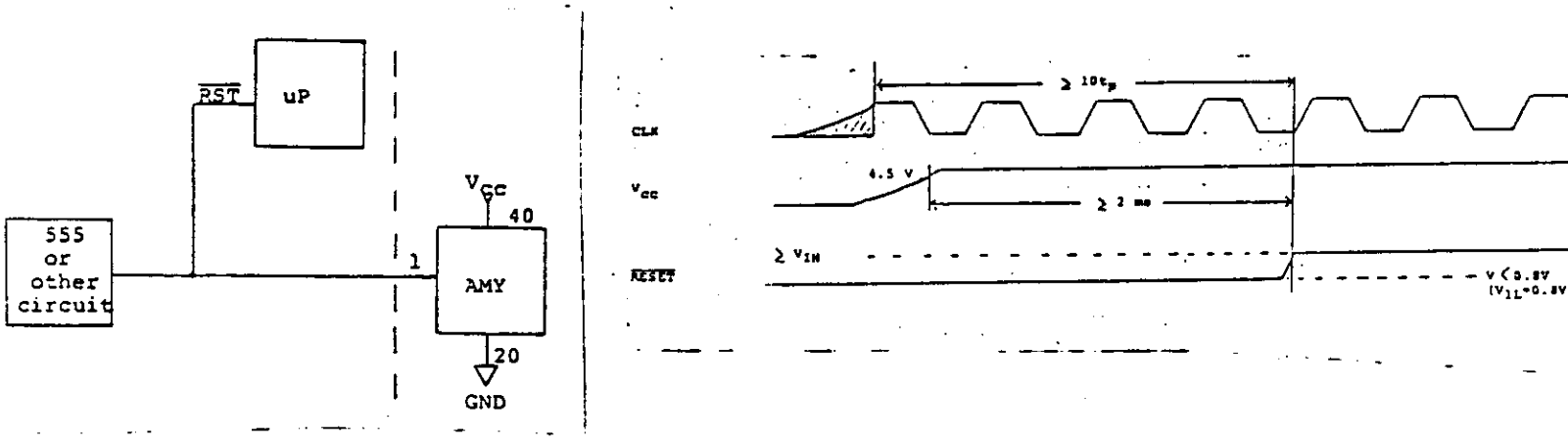
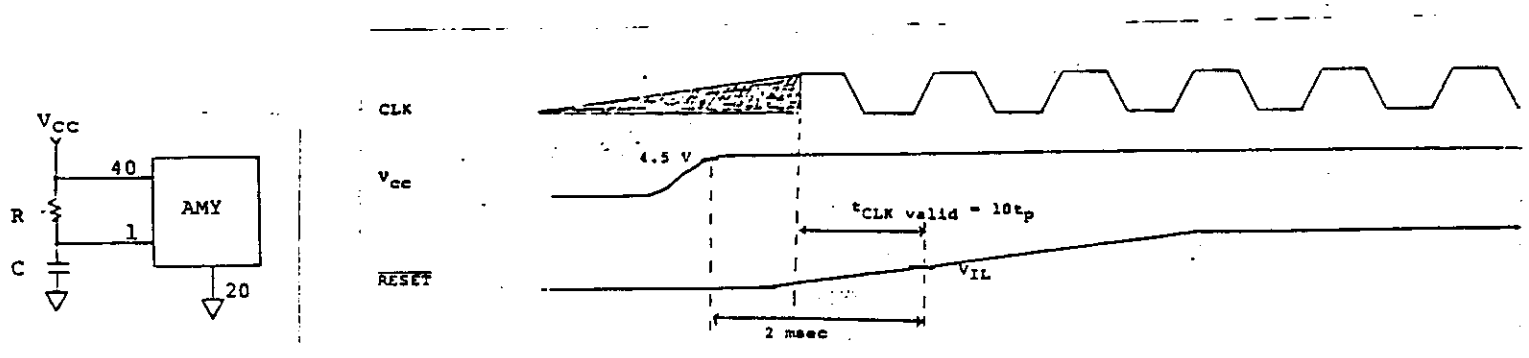


Figure 8. RESET with Standard uP System Reset Circuit



Note: RC requirements depend on V_{CC} rise time.

Figure 9. RESET with RC (see Appendix II).

7.4 Other User Accessible Registers and RAM Areas

AMY also contains other internal registers which are loaded by sending various commands to the AMY Command register. These registers are the System Options register, the System Control register, and the Last Harmonic Pair register (see Sections 7.5.5, 7.5.6, and 7.5.8, respectively).

Other AMY commands pass data to or from AMY RAM areas. These RAM areas include the Voice RAM, the Harmonic RAM, and the Noise RAM. The VRAM contains the current fundamental frequency, fundamental frequency breakpoint, and the voice type. The HRAM contains the current harmonic amplitude and the harmonic amplitude breakpoint. Initial conditions of the NRAM may be loaded to obtain specific bandlimited white noise statistics.

In general, all registers are loaded directly with a single one byte write operation (even the SOR, SCR, and LHPR are loaded from operand data in the command byte). Alternately, RAM areas are read/written to indirectly by using Reg A, B, and C as data buffers.

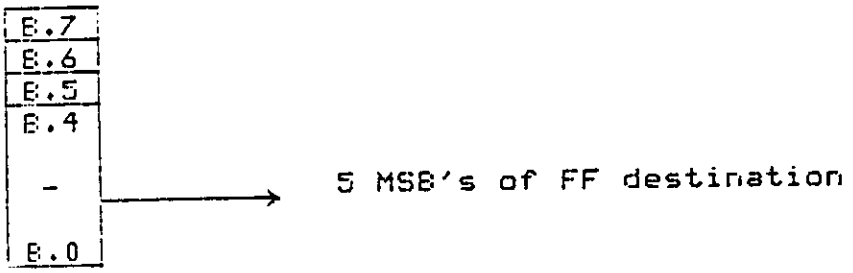
7.5 Command Descriptions

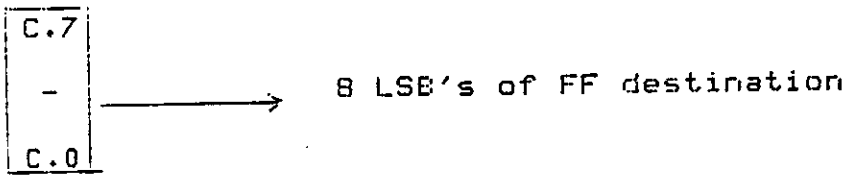
7.5.1 Write Fundamental Frequency Breakpoint Command (Write FFBP)

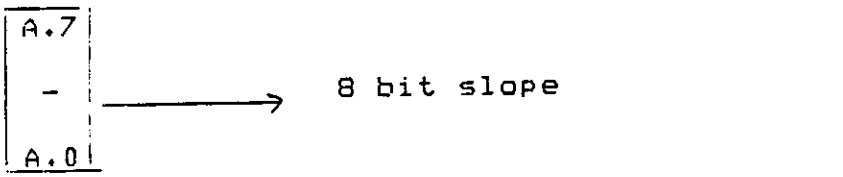
Command:

0	0	0	0	1	V2	V1	V0

This command loads a new fundamental frequency slope and destination (FFBP) for the desired voice into the voice RAM. This is done indirectly by loading Reg A, B, and C before the command is issued. V2, V1 and V0 are the voice pointer bits; that is, if V2 = V1 = V0 = 0, then Voice 0's FFBP (slope and destination) will be loaded. If V2 = V1 = 0 and V0 = 1, then Voice 0's FFBP will be modified. The register data format for this command is:







If the slope (Reg A) is zero when the Write FFBP command is issued, the destination will be loaded immediate into the FF current value field of the VRAM. It will remain there until another Write FFBP command is issued.

The slope and destination data are be loaded into the A, B, and C registers before the WR FFBP command is executed.

Slope:

Register A:

A.7	A.6	A.5	A.4	A.3	A.2	A.1	A.0
Sign	Exponent			Mantissa			

Bits 7,4-0: Increment Value
(from -31/2048 to 31/2048 of a semitone)

A.7	A.4	A.3	A.2	A.1	A.0	Semitone Increment
0	1	1	1	1	1	31/2048
			.			.
			.			.
			.			.
0	0	0	0	1	0	2/2048
0	0	0	0	0	1	1/2048
0	0	0	0	0	0	Zero slope.
1	1	1	1	1	1	-1/2048
1	1	1	1	1	0	-2/2048
			.			.
			.			.
			.			.
1	0	0	0	0	1	-31/2048
1	0	0	0	0	0	Not allowed

Bits 6-5: Subsample Rate Control

A.6	A.5	INCREMENT RATE
0	0	Add once every 128 sample periods
0	1	Add once every 32 sample periods
1	0	Add once every 8 sample periods
1	1	Add once every 2 sample periods

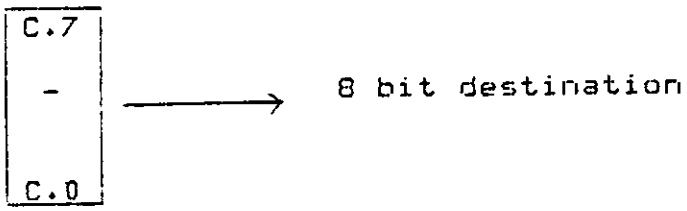
Destination:

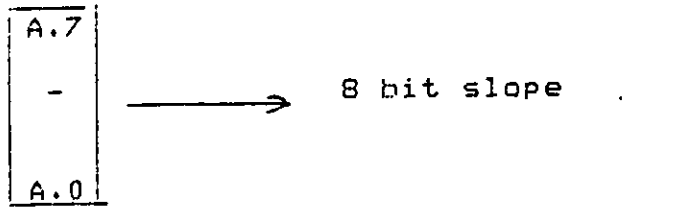
There are 8196 possible destination values which cover a range of 128 semitones (1/64 of a semitone resolution).

7.5.2 Write Harmonic Amplitude Breakpoint Command (Write HABP)

Command: 0 1 H5 H4 H3 H2 H1 H0

This command loads a new Harmonic Amplitude slope and destination value (HABP) for the specified harmonic into the Harmonic RAM. The harmonic number is specified by the least significant 6 bits of the command byte (H5-H0). The operation is performed indirectly by loading Reg A and C before the command is issued. Reg B is not used in this command. The register format for this command is:





If the slope byte (Reg A) is zero when the command is issued, the destination will be loaded immediate into the HA current value field of the Harmonic RAM. It will remain at that value until another Write HABP command is issued. This mode is most useful in the "cold start" software routine immediately after power up of AMY, since all harmonic amplitudes may be loaded immediate to zero before the SEQRUN bit is set (see Section 7.5.6).

Slope:

Register A: A.7 A.6 A.5 A.4 A.3 A.2 A.1 A.0

Sign Exponent 5 bit Mantissa

Bits 7,4-0: Increment Value
(from -31/128 to 31/128 of a decibel)

A.7	A.4	A.3	A.2	A.1	A.0	Increment (decibels)
0	1	1	1	1	1	31/128
			.			.
			.			.
			.			.
0	0	0	0	1	0	2/128
0	0	0	0	0	1	1/128
0	0	0	0	0	0	Zero Slope
1	1	1	1	1	1	-1/128
1	1	1	1	1	0	-2/128
			.			.
			.			.
			.			.
1	0	0	0	0	1	-31/128
1	0	0	0	0	0	Not allowed

Bits 6-5: Subsample Rate Control

A.6	A.5	Increment Rate
0	0	Add once every 128 sample periods
0	1	Add once every 32 sample periods
1	0	Add once every 8 sample periods
1	1	Add once every 2 sample periods

Destination:

There are 256 possible destination values covering a 64 dB dynamic range (1/4 of a decibel resolution).

7.5.3 Read Fundamental Frequency Current Value (RD FFCV)

Command: 0 0 0 1 1 V2 V1 V0

This command instructs the AMY sequencer to read, from the Voice RAM, the current value field for the voice specified by the 3 LSB's of the command (V2, V1, V0) and load its contents into the B and C registers where it can be examined by the user. Reg A is not used in this command. The register-format is as follows:

B.7
B.6
B.5
B.4
-
B.0

5 MSB's of Current FF value

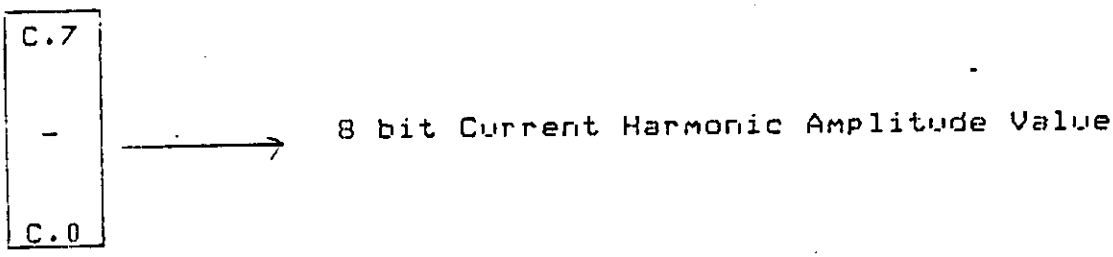
C.7
-
C.0

8 LSB's of current FF value

7.5.4 Read Harmonic Amplitude Current Value (RD HACV)

Command: 1 1 H5 H4 H3 H2 H1 H0

This command instructs the AMY sequencer to read the current value of the harmonic (specified by the 6 LSB of the command byte) into Reg C. The user may then read Reg C for the current amplitude of the specified harmonic. The A and B registers are not used even though Reg B is modified by this command.



7.5.5 Write System Options Register (WR SOR)

Command: 0 0 1 0 SO3 SO2 SO1 SO0

This command allows the user to select 4 options in AMY operation. The 4 options bits, described below, are loaded directly from the least significant 4 bits of the command byte. Reg A, B, and C are not used in this command.

SO3 →	40/$\overline{64}$ Harmonics	Selects 40 or 64 harmonics
SO2 →	$\overline{\text{SUM}}$ MODE	Selects individual voice output or sum of all voices output format
SO1 →	INT MODE	Select interrupt or ready mode
SO0 →	ALE MODE	Select ALE mode or Address pin mode

SO3	SO2	SO1	SO0	AMY Mode
X	X	X	0	ADDRESS PIN Mode
X	X	X	1	ALE Mode
X	X	0	X	READY Mode
X	X	1	X	INTERRUPT Mode
X	0	X	X	SUM Mode
X	1	X	X	INDIVIDUAL Mode
0	X	X	X	64 HARMONICS Mode
1	X	X	X	40 HARMONICS Mode
0	0	0	0	RESET State - Initialize Default (ADR pin, READY, SUM and 64 HARMONICS)

Table 4. System Options Register Selection.

Notes:

1. In ADDRESS PIN mode, Table 4 shows how register selection is accomplished by using the A1 and A0 pins.

2. In ALE mode, the user must put the address information on the data bus (DB1 and DB0) during the ALE strobe time. (In multiplexed bus processors, like the 8051, this occurs shortly before the RD or WR strobe times.)

sample rate equation

7.5.6 Write System Control Register (WR SCR)

Command: 0 0 1 1 X X SC1 SC0

This command allows the user to stop the AMY output accumulation process thus holding the output bus to zero, avoiding power up glitches. It also allows the user to place AMY in a special "noise initialize mode." When the WR SCR command is sent, the least significant 2 bits of the command byte are loaded into the SCR. Reg A, B, and C are not used in this command.

SC1 ——→ NZINIT Select Noise RAM mode or Last Harmonic Pair mode

SC0 ——→ SEQRUN Software Reset

SC1	SC0	AMY Mode
X	0	HALT Mode
X	1	SEQUENCER RUN Mode
1	X	Initialize Noise RAM
0	X	NOISE RUN Mode

Table 5. System Control Register Selection.

Notes:

1. The Sequencer must be running to generate digital sound on the SAMP bus. (In HALT mode, if OE = "0", SAMP(14-0) = "0", SAMP15 = "1")

2. In HALT mode, AMY resets the phase of all harmonic oscillators to zero (for selected voices only).

3. Initialization of the Noise RAM may be done in the HALT or the SEQUENCER RUN mode.

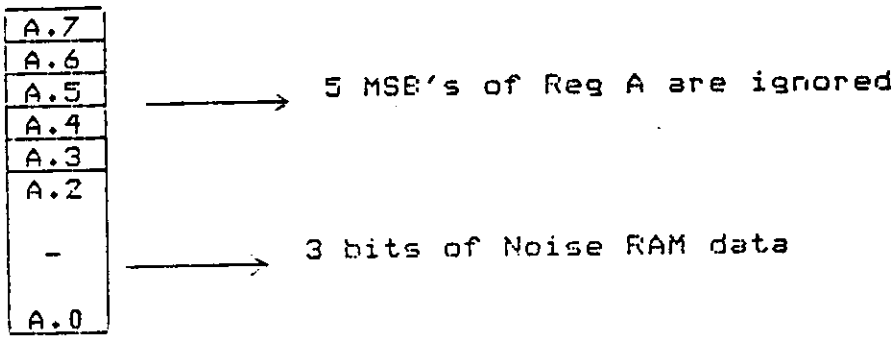
4. When in NOISE RUN mode, both Noise Generators are running and may be selected for use in a particular "Noise Voice" (see Write Voice Type command, Section 7.5.9).

7.5.7 Write Noise RAM Command

Command:	1	0	N5	N4	N3	N2	N1	N0

Note: To use this command, the NZINIT bit in the SCR must be set.

This command loads data from Reg A into the Noise RAM. The address of the Noise RAM is specified in the least significant 6 bits of the command byte. Valid Noise RAM addresses range from 00 to 1D Hex (Noise Generator 0) and from 28 to 3F Hex (Noise Generator 1).
The Noise RAM takes up a total of 54 address locations. Loading Noise RAM data to addresses between 1E and 27 Hex is not recommended. Each of the 54 valid Noise RAM locations may be loaded with a 3 bit value. The value is specified by the least significant 3 bits of Reg A. Reg A must be loaded with the proper data before the WR Noise RAM command is issued. See Section 8.2 for Initialization flow chart.



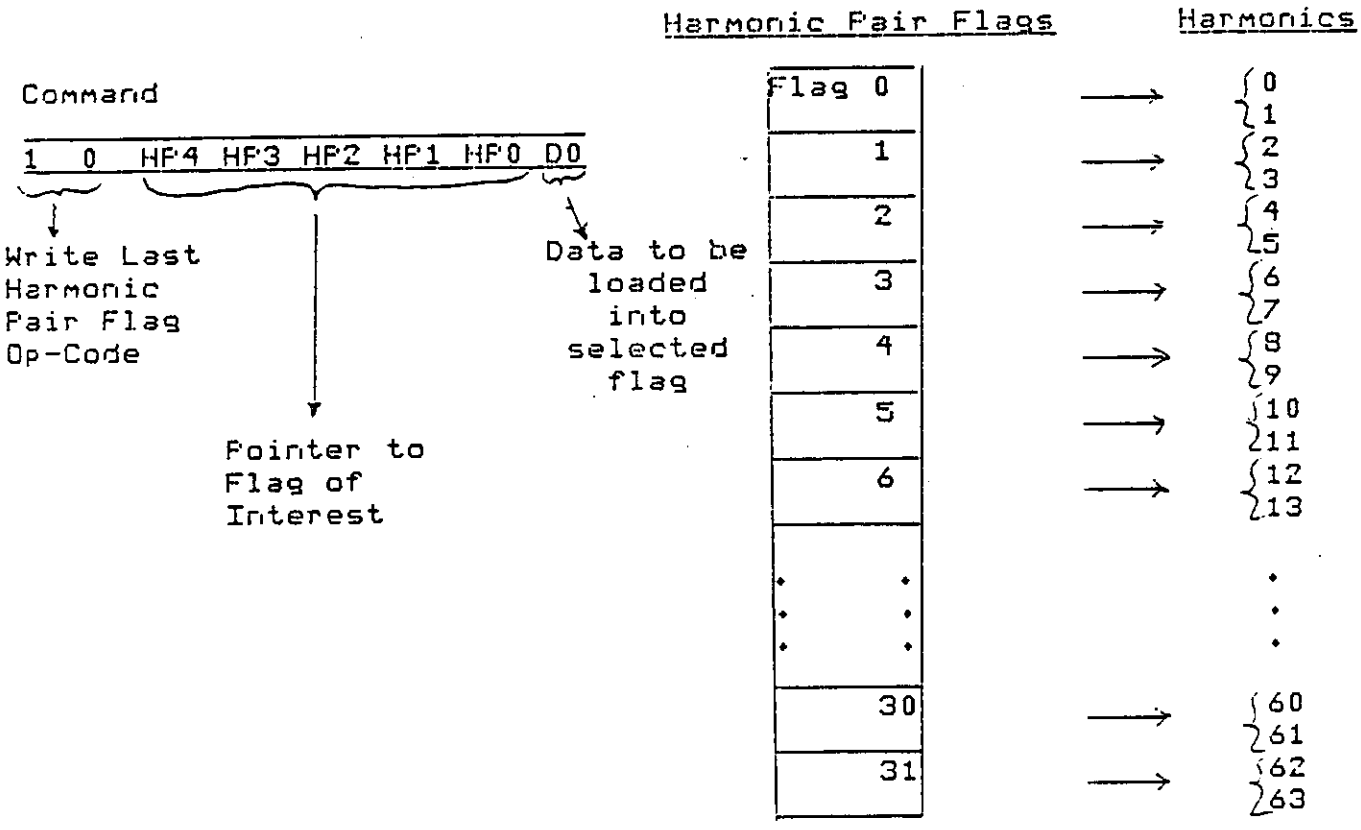
7.5.8 Write Last Harmonic Pair Flag Command

Command: 1 0 HP4 HP3 HP2 HP1 HP0 D0

Note: To use this command, the NZINIT bit in the SCR must first be cleared.

This command allows the user to specify the number of harmonics allocated to each voice. There are a maximum of 8 voices and a maximum of either 40 or 64 harmonics (depending on the state of the 40/64 bit in the SCR). Harmonics must be allocated in groups of 2 or as harmonic pairs. Harmonics 0 and 1 are always assigned to Voice 0. Each pair of harmonics has a Last Harmonic Pair flag which determines whether or not these two harmonics are the last two harmonic of some voice. Therefore, there are 32 such flags. A maximum of 8 of these 32 flags should be set at any one time (since we are limited to 8 voices).

For a single voice of 64 harmonics, all last harmonic pair flags would be set to zero except the last one which is last harmonic pair flag 31. The HP4-HP0 field in the command byte specifies which flag is to be loaded. The LSB of the command byte (D0) specifies whether the flag is to be cleared or set. The 32 flags power up in a random state and thus all 32 must be set/cleared after power up to define the number of harmonics per voice. Reg A, B, and C are not used by this command.

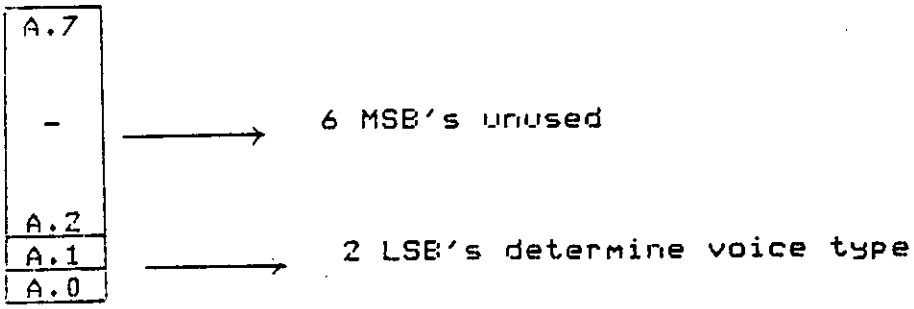


Example: If all flags are reset except for Flag 3 = Flag 31 = 1, AMY will be set up for 2 voices. Voice 0 will have 8 harmonics (0 through 7) and Voice 1 will have 56 harmonics (8 through 63).

7.5.9' Write Voice Type Command

Command:	0	0	0	1	0	V2	V1	V0

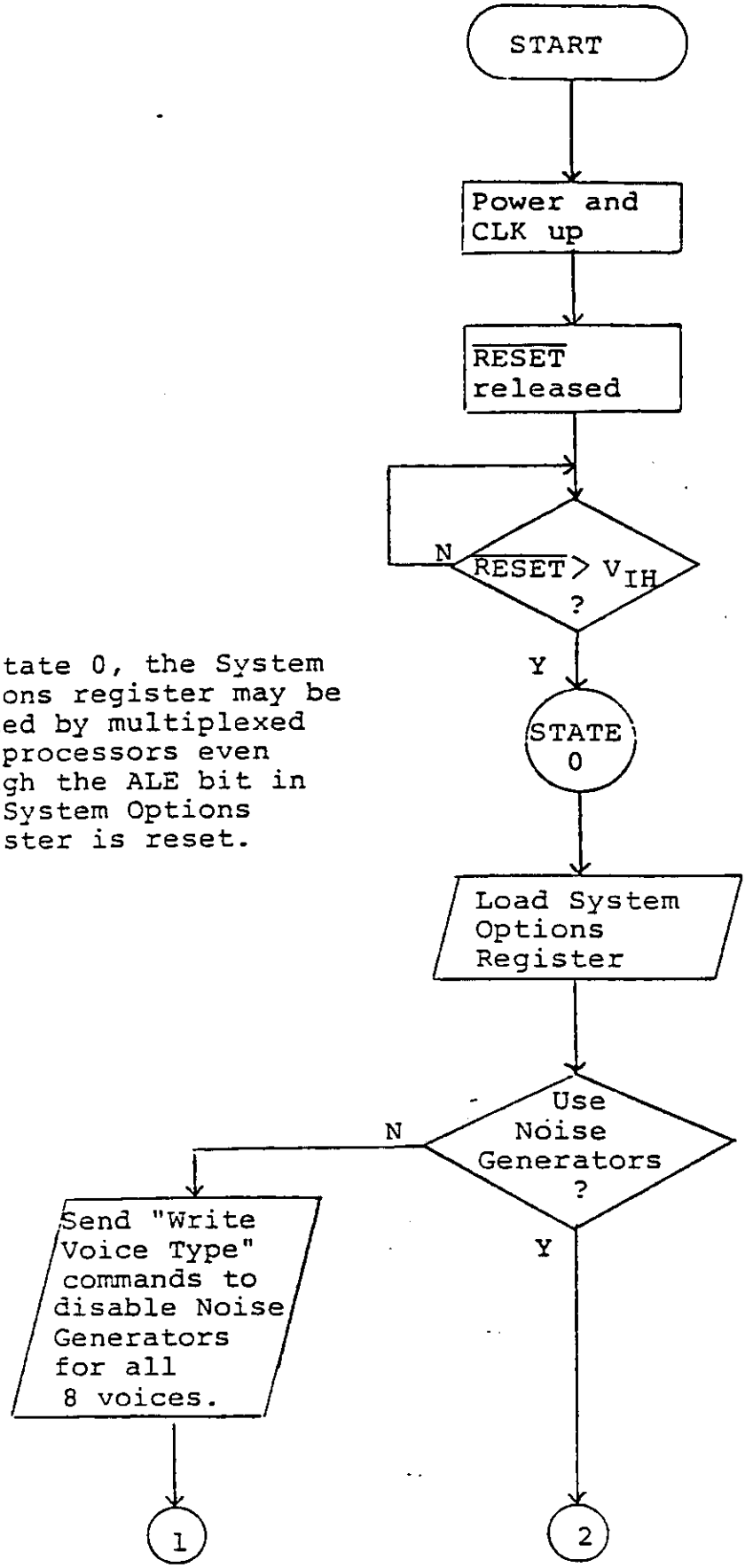
Each voice may be assigned as a Harmonic Voice or as one of two different Noise Source Based Voices. The desired voice is selected by the least significant 2 bits of the command byte. The least significant 2 bits of Reg A determine the "type" of voice desired. Reg A must be loaded before the command is issued according to the following convention (Reg B and C are not used):



A.1	A.0	Type
0	0	Harmonic
0	1	Noise Type 0
1	0	Noise Type 1
1	1	~~Undefined~~ Illegal

8.2 Initialization Flow Chart

When $\overline{RESET}$ = 1, assuming the conditions of the previous page have been met, AMY is in state 0 of the following flow chart:

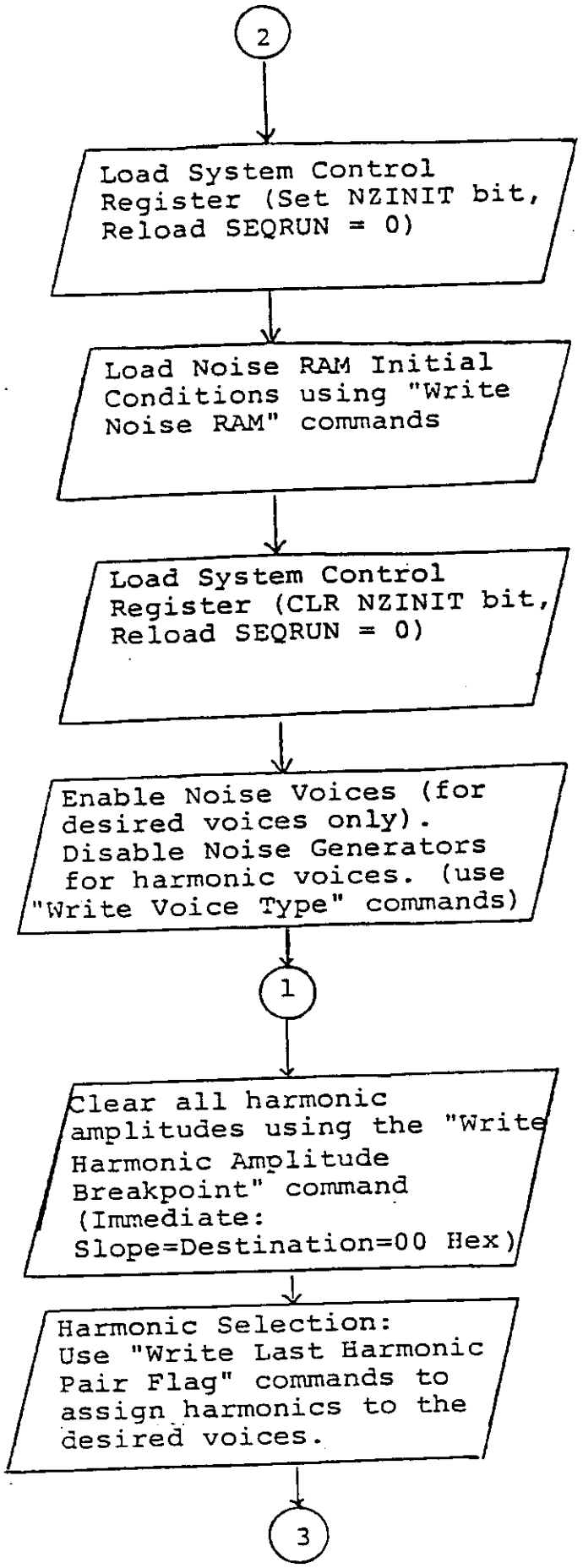


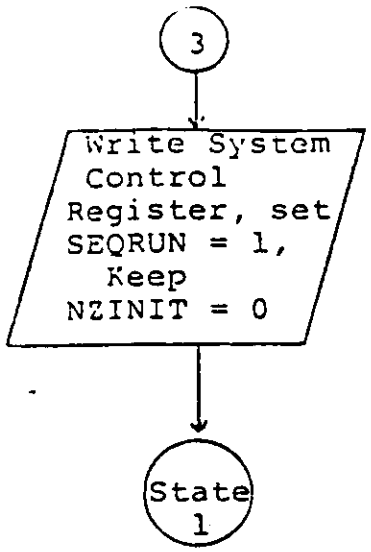
$\overline{RESET}$ held $< V_{IL}$

During the time $\overline{RESET}$ is below V_{IL} = 0.8V, the System Options register and System Control register bits are all cleared.

In State 0, the System Options register may be loaded by multiplexed bus processors even though the ALE bit in the System Options register is reset.

1. ALE mode must be selected if using multiplexed bus uP like the 8051.
2. The 40/$\overline{64}$ bit should be loaded for desired sample rate.
3. The INT bit selects desired operation of the INT/RDY pin.
4. The $\overline{SUM\ MODE}$ bit should be cleared unless Individual voice outputs are desired.


2
Load System Control Register (Set NZINIT bit, Reload SEQRUN = 0)
Setting NZINIT stops the 2 Noise Generators They can be initialize when NZINIT = 1.
Load Noise RAM Initial Conditions using "Write Noise RAM" commands
Load System Control Register (CLR NZINIT bit, Reload SEQRUN = 0)
Noise Generators start running.
Enable Noise Voices (for desired voices only). Disable Noise Generators for harmonic voices. (use "Write Voice Type" commands)
1
Clear all harmonic amplitudes using the "Write Harmonic Amplitude Breakpoint" command (Immediate: Slope=Destination=00 Hex)
Harmonic Selection: Use "Write Last Harmonic Pair Flag" commands to assign harmonics to the desired voices.
3



Although all oscillators are now running and the digital output bus (SAMP0-15) are no longer disabled, the SAMP bus will remain at the "Zero" level since all harmonic amplitudes have been loaded immediate to zero.

Run state

Once the user is in the RUN STATE (State 1), voices may be constructed by first loading the fundamental frequency immediate to some start value and then ramping up/down the Harmonic amplitudes (even the fundamental frequency, if desired). In State 1, an unlimited number of harmonic and fundamental frequency breakpoints may be loaded. Maximum bandwidth of breakpoints is approximately 200,000 BP/sec (essential for peaks in activity). Also, in State 1, the noise generators may be stopped and the Noise RAM reloaded (when the Noise Generator starts running again, the statistics of the noise may change). The number of harmonics per voice may also be modified. The user may change a voice's type, or may read current values of fundamental frequency for any voice or harmonic amplitude for any harmonic. When drastic changes are to be made it is recommended that the user return to State 0 by loading SEQRUN = 0 with the "Write System Control register Command. In some cases, it may be desirable to "Ramp" all harmonic amplitudes to "zero" before loading SEQRUN = 0 (to avoid a "click").

8.3 Summary

Initialization of AMY requires the following steps:

1. Loading System Options register.

   a. Select 40 or 64 harmonics where the sample rate = $\frac{1}{2 * \#\ \text{harmonics} * t_p}$, t_p = clock period

      Example: 64 harmonics with a 4 MHz clock rate results in a 31.25 KHz sample rate.

   b. Select ALE or Address Pin mode. If ALE mode is desired, the A0 and A1 pins should be tied to ground.

   c. Select INT/RDY pin function. If INT bit = 1, the INT/RDY pin will issue a single clock pulse wide interrupt pulse at the completion of all commands. If INT bit = 0, the INT/RDY pin will function as a Ready pin. In the READY mode, the INT/RDY pin will go low (logic 0) immediately upon receipt of a command and return high (logic 1) when the command has been completely executed (see Figure 10).

   d. Select between SUM mode (all voices added together and output once each sample period) or INDIVIDUAL mode (all voices output separately). There will be N output samples per sample period in the INDIVIDUAL mode - N is the number of voices enabled).

2. Defining voices using the "Write Last Harmonic Pair Flag" command.

3. Clearing all harmonic amplitudes to zero before setting SEQRUN = 1.

4. Loading initial conditions into Noise RAM using Write System Control register command and Write Noise RAM command.

5. Assigning each voice an initial voice type.

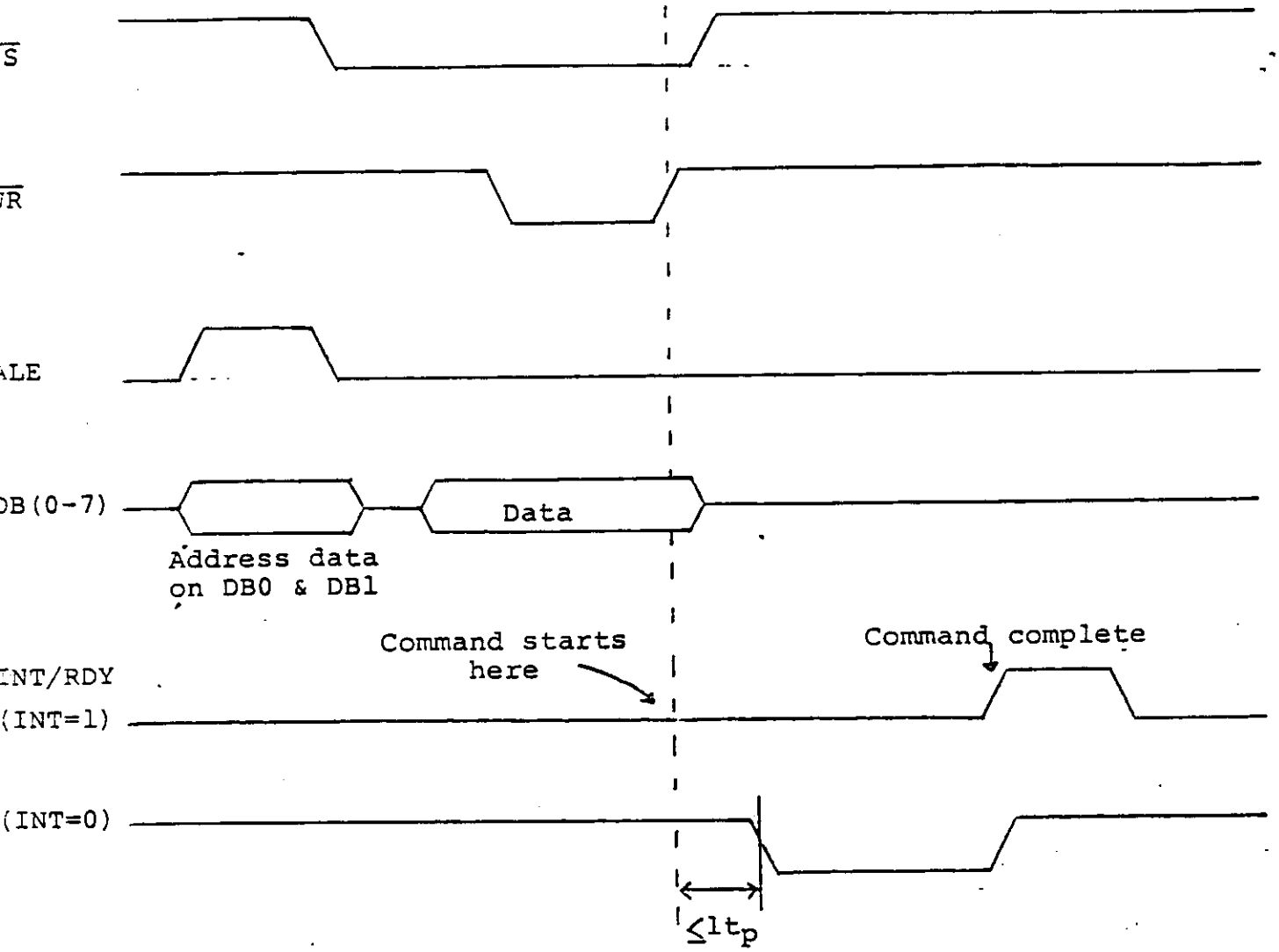


Figure 10. INT/RDY Pin Timing

9. MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	-65 to +150°C
Ambient Temperature Under Bias	0 to +70°C
Voltage at any Pin Relative to Ground	-0.5 to +7 V
Power Dissipation	750 mW

10. CAPACITANCES

Ambient Temperature Parameters: $T_A = 25^oC$; V_{CC} = GND = 0 V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

11. D.C. CHARACTERISTICS

Ambient Temperature Parameters: T_A = 0 to 70°C, Vcc = +5 V ± ~~10%~~ 5%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100uA
I_L	Input Leakage Current		10	uA	0 ≤ Vin ≤ Vcc
I_O	Output Leakage Current		10	uA	0.45≤Vout≤Vcc

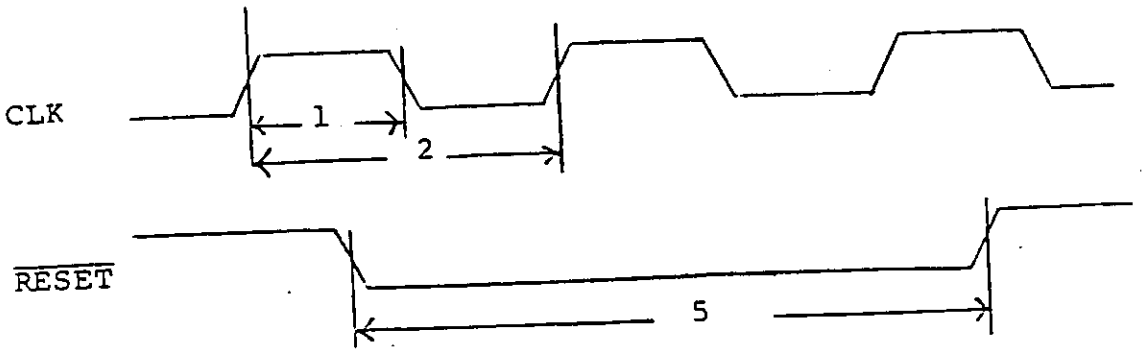
12. A.C. CHARACTERISTICS

12.1 CLOCK & RESET

T_A=0 to 70°C
V_{cc}=5 V ±10%

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_p	Clock Period	200	500	nS	
2	t_ϕ	Clock High Time	$0.4t_p$	$0.6t_p$		
3	t_{cr}	Clock Rise Time		30	nS	10% to 90%
4	t_{cf}	Clock Fall Time		30	nS	10% to 90%
5	t_{rpw}	$\overline{\text{RESET}}$ Pulse Width	$2t_p$			

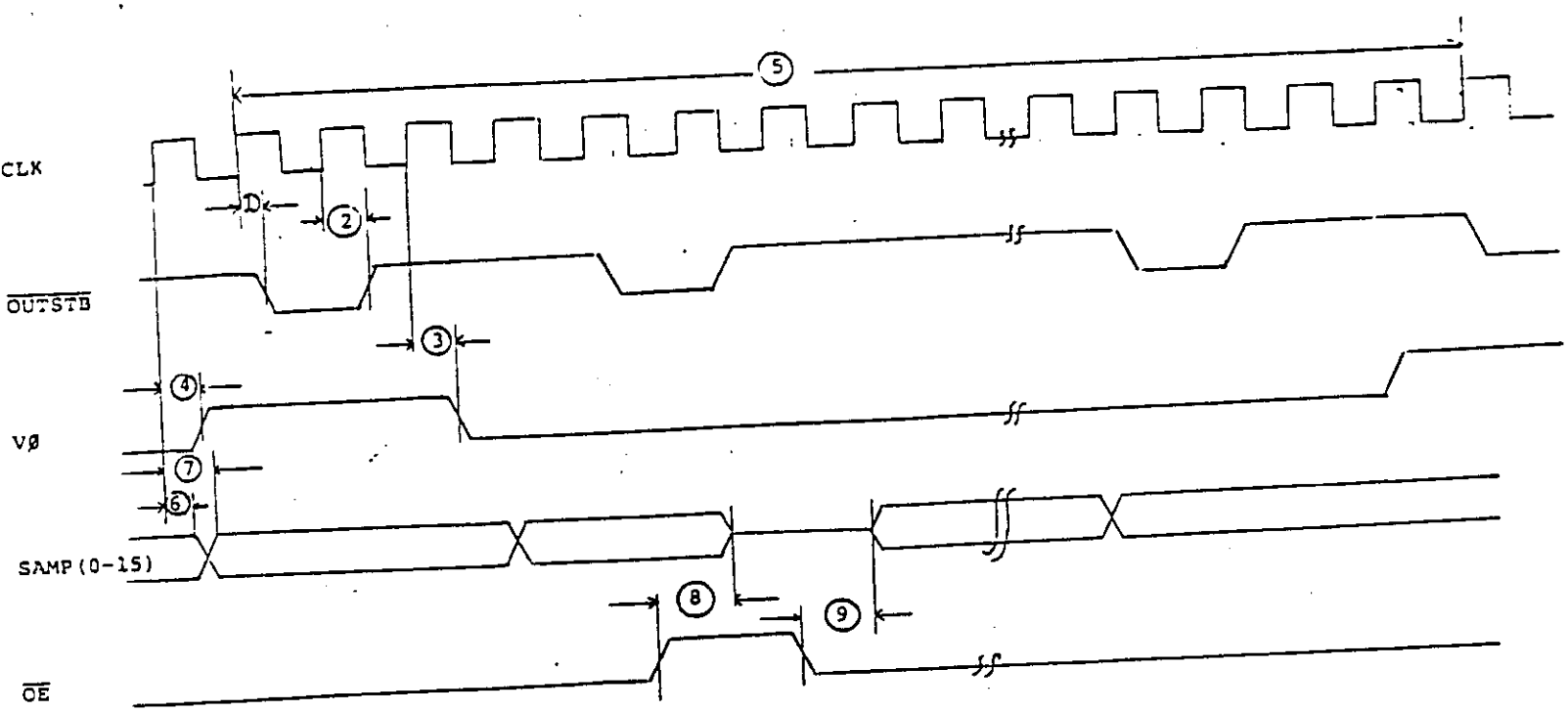
Note: $\overline{\text{RESET}}$ should be held low (less than V_{IL}=0.8 Volts) during power up of the AMY chip. It should remain low for greater than or equal to 2 msec after power meets spec (4.5 to 5.5 Volts).



12.2 OUTPUT SECTION

T_A=0 to 70°C, C_L=150 pF unless noted
V_{cc}=5 V ±10%, 2 MHz≤f_{clk}≤5 MHz

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_{col}	CLK to $\overline{OUTSTB}$ Low	Ø	150	nS	
2	t_{cot}	CLK to $\overline{OUTSTB}$ High	0	150	nS	
3	t_{cvt}	CLK to V0 Falling Edge	0	150	nS	
4	t_{cvl}	CLK to V0 Rising Edge	Ø	150	nS	
5	t_s	Sample Period				
		1) 40 Harmonic	$80t_p$	$80t_p$		$t_p=1/f_{clk}$
		2) 64 Harmonic	$128t_p$	$128t_p$		
6	t_{sh}	SAMP(0-15) Data Hold Time From CLK	20		nS	
7	t_{cshl}	CLK to SAMP(0-15) Data Valid		150	nS	OE≤V_{IL}
8	t_{csf}	$\overline{OE}$ Rising Edge to SAMP(0-15) Output Float	0	150	nS	
9	t_{cse}	$\overline{OE}$ Falling to SAMP(0-15) Outputs Valid	0	150	nS	



Output Timing Diagram - Individual Mode

Notes:

1. VØ goes active one time (for several successive clock periods) each sample period.

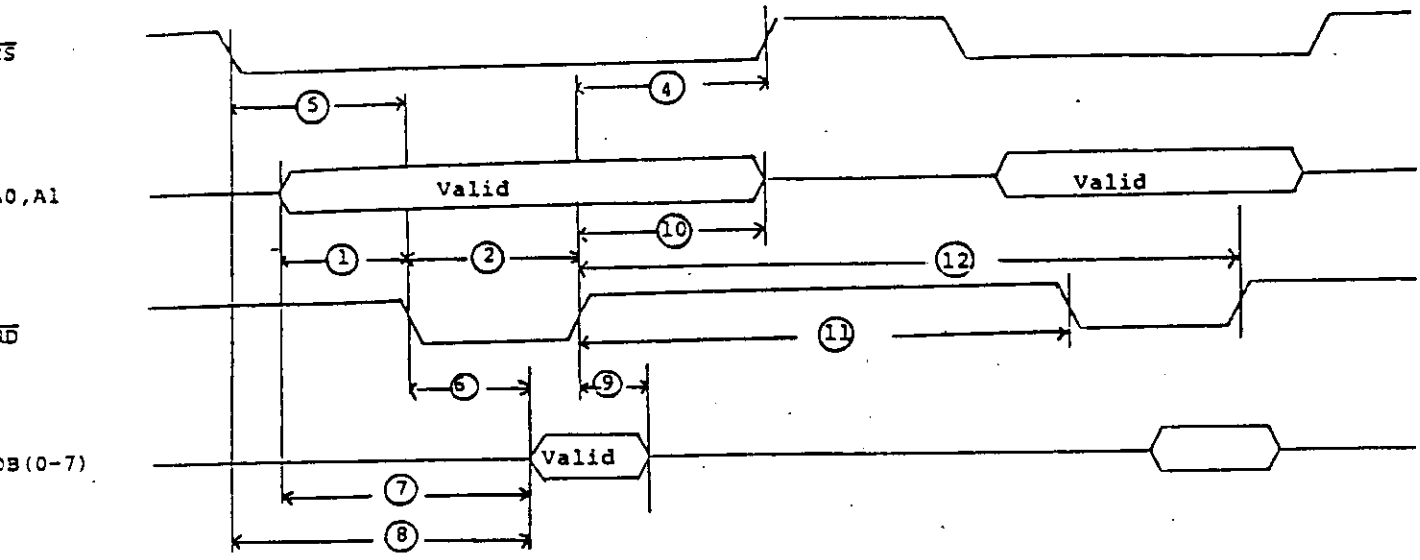
2. The number of $\overline{\text{OUTSTB}}$ pulses in one sample period is equal to the number of Voices in use. The time between $\overline{\text{OUTSTB}}$ pulses depends on the number of harmonics allocated to each voice. (ie, in the above diagram, Voice 1 has 2 harmonic oscillators assigned to it. - In general, if Voice N has 2 harmonics assigned to it, then Voice((N-1) modulo M) samples are present on the samp bus for 2.2 clock periods (M = # Voice assigned)

12.3 SYSTEM BUS INTERFACE - Read Amy and Write Amy (Address Pin and ALE mode).

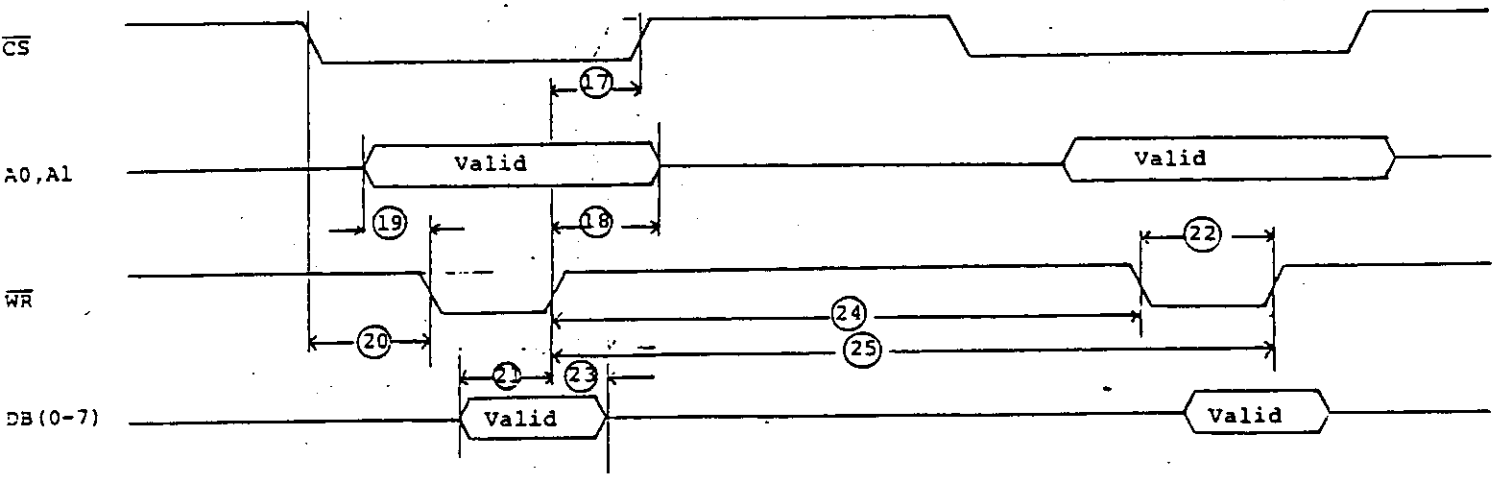
Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_{ar}	Address valid to $\overline{RD}$	Ø		nS	
2	t_{rr}	$\overline{RD}$ Pulse Width	200		nS	
3	t_{af}	ALE Float Time	10	100	nS	
4	t_{chr}	$\overline{CS}$ Hold Time after $\overline{RD}$	Ø		nS	
5	t_{cr}	$\overline{CS}$ Active to $\overline{RD}$	Ø		nS	
6	t_{rd}	Read Access Time	150		nS	
7	t_{ao}	Address to Data Valid	150		nS	
8	t_{cd}	$\overline{CS}$ Active to Data Valid	150		nS	
9	t_{rdh}	Data Bus Hold Time after $\overline{RD}$		10	nS	
10	t_{ahr}	Address Hold Time after $\overline{RD}$	Ø		nS	
11	t_{rdead1}	$\overline{RD}$ Dead Time (address pin mode)	100		nS	
12	t_{cycr1}	Read Cycle Time (address pin mode)	300		nS	
13	t_{rdf}	Read Float Time ($\overline{RD}$ to DB(0-7) Float)	10	100	nS	
14	t_{rdead2}	$\overline{RD}$ Dead Time (ALE Mode)	250		nS	
15	t_{apw}	ALE Pulse width	50		nS	
16	t_{cycr2}	ALE Mode Read Cycle Time	450		nS	

SYSTEM BUS INTERFACE (Cont.)

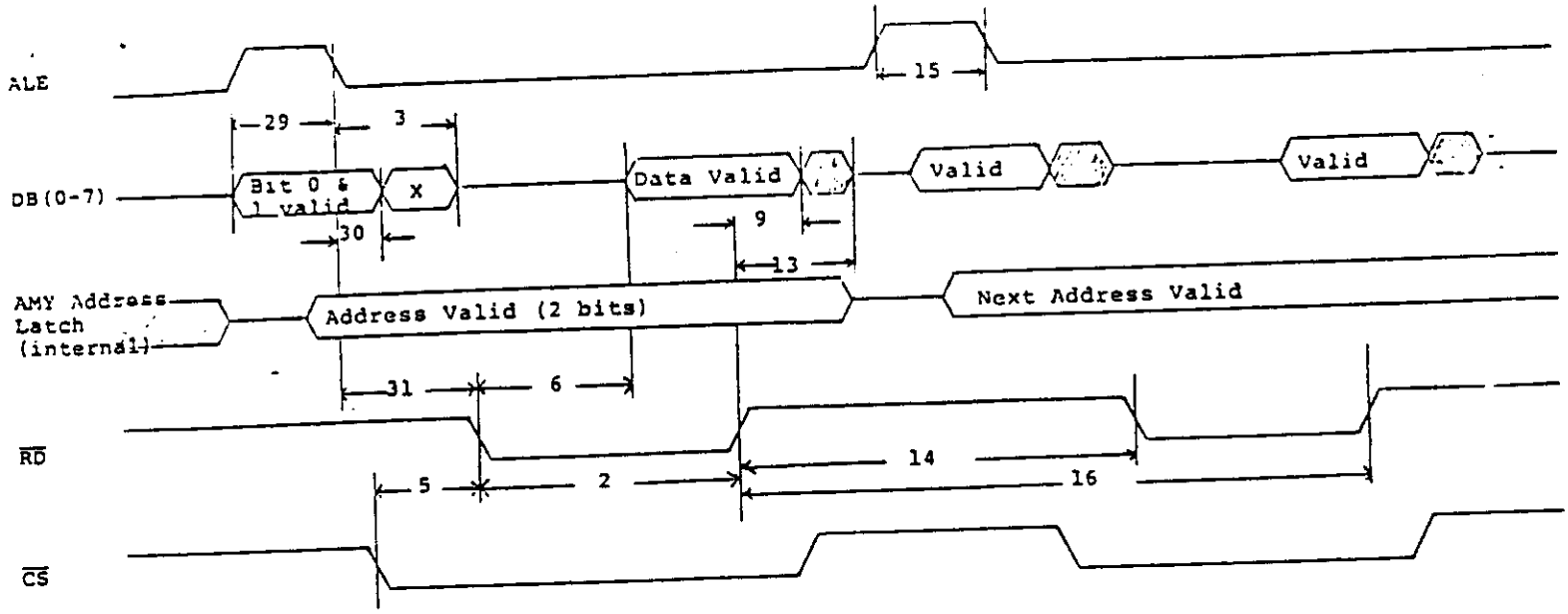
Number	Symbol	Parameter	Min	Max	Units	Comments
17	t_{chw}	$\overline{CS}$ Hold Time after $\overline{WR}$	Ø		nS	
18	t_{ahw}	Address Hold Time after $\overline{WR}$	Ø		nS	
19	t_{aw}	Address setup Time to $\overline{WR}$		50	nS	
20	t_{cw}	$\overline{CS}$ Setup Time to $\overline{WR}$	Ø		nS	
21	t_{dw}	Data Setup Time to $\overline{WR}$		50	nS	
22	t_{ww}	$\overline{WR}$ Pulse Width	200		nS	
23	t_{wd}	Data Hold Time to $\overline{WR}$	Ø		nS	
24	t_{wdead1}	Write Dead Time (Address)	100		nS	
25	t_{cycw}	Write Cycle Time (Address)	300		nS	
26	t_{alewr}	ALE to $\overline{WR}$	50		nS	
27	$t_{cycwale}$	Write Cycle Time (ALE)	400		nS	
28	t_{wdead2}	Write Dead Time (ALE)	200		nS	
29	t_{dwa}	Data Valid to ALE falling edge		50	nS	
30	t_{wda}	Data hold after ALE falling edge	Ø		nS	
31	t_{alerd}	ALE Falling edge to $\overline{RD}$ Falling edge	20		nS	



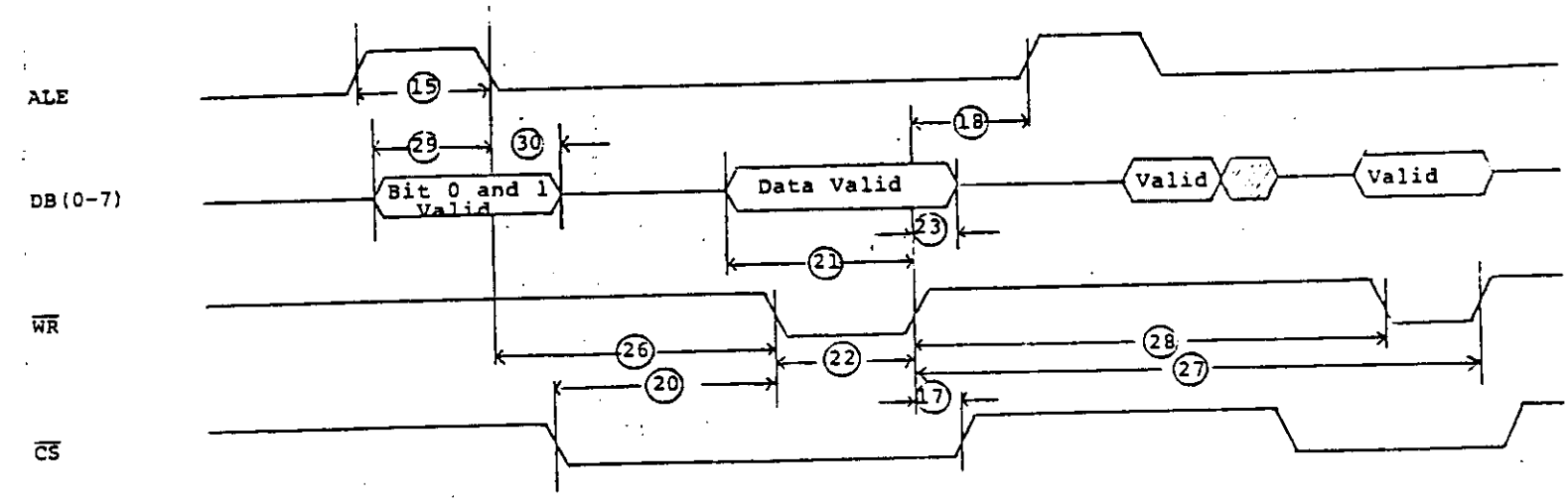
Address Pin Mode (ALE pin grounded, ALE bit in SOR = "Ø")
Read AMY Cycle



Address Pin Mode (ALE pin grounded, ALE bit in SOR = "Ø")
Write AMY Cycle



ALE Mode (AØ and A1 grounded, ALE bit in SOR = "1")
Read AMY Cycle



ALE Mode (AØ and A1 grounded, ALE bit in SOR = "1")
Write AMY Cycle

APPENDIX I.

Table A shows the 13 bit ~~Atari Tone (TTP)~~ Tone values which correspond to full semitone steps on a piano keyboard. For example, Note A (440 Hz) will be reached if a fundamental frequency envelope reaches a destination value of 5004 Decimal (138C Hex). At a 4 MHz clock rate the actual frequency will be 440.04 Hz. The MSB and LSB fields show the Decimal values of the Destination MSB and LSB fields corresponding to the ~~TTP~~ Atari Tone value.

Table B is in the same format as Table A, but the "Note" field was dropped ~~since the values listed are actually~~ "in between" 2 semitones (or notes on a piano). Table B shows that the actual frequency resolution at 440 Hz is approximately 0.4 Hz (1.5 cents).

Table C shows actual semitone/sec and decibel/sec slopes achieved by various 8 bit slope values. The M (mantissa) and E (exponent) fields are separated to give a feeling for the exponential coding scheme of slope byte. (Data valid for 4 MHz clock frequency and 64 harmonic mode).

TABLE A

Atari Tone	MSB	LSB	FREQ	NOTE
140	0	140	5.4	F
204	0	204	5.7	F#/Gb
268	1	12	6.1	G
332	1	76	6.4	G#/Ab
396	1	140	6.8	A
460	1	204	7.2	A#/Bb
524	2	12	7.7	B
588	2	76	8.1	C
652	2	140	8.6	C#/Db
716	2	204	9.1	D
780	3	12	9.7	D#/Eb
844	3	76	10.3	E
908	3	140	10.9	F
972	3	204	11.5	F#/Gb
1036	4	12	12.2	G
1100	4	76	12.9	G#/Ab
1164	4	140	13.7	A
1228	4	204	14.5	A#/Bb
1292	5	12	15.4	B
1356	5	76	16.3	C
1420	5	140	17.3	C#/Db
1484	5	204	18.3	D
1548	6	12	19.4	D#/Eb
1612	6	76	20.6	E
1676	6	140	21.8	F
1740	6	204	23.1	F#/Gb
1804	7	12	24.5	G
1868	7	76	25.9	G#/Ab
1932	7	140	27.5	A
1996	7	204	29.1	A#/Bb
2060	8	12	30.8	B
2124	8	76	32.7	C
2188	8	140	34.6	C#/Db
2252	8	204	36.7	D
2316	9	12	38.8	D#/Eb
2380	9	76	41.2	E
2444	9	140	43.6	F
2508	9	204	46.2	F#/Gb
2572	10	12	49	G
2636	10	76	51.9	G#/Ab
2700	10	140	55	A
2764	10	204	58.2	A#/Bb
2828	11	12	61.7	B
2892	11	76	65.4	C
2956	11	140	69.3	C#/Db
3020	11	204	73.4	D
3084	12	12	77.7	D#/Eb
3148	12	76	82.4	E
3212	12	140	87.3	F
3276	12	204	92.5	F#/Gb

TABLE A (continued)

Atari Tone	MSB	LSB	FREQ	NOTE
3340	13	12	98	G
3404	13	76	103.8	G#/Ab
3468	13	140	110	A
3532	13	204	116.5	A#/Bb
3596	14	12	123.4	B
3660	14	76	130.8	C
3724	14	140	138.6	C#/Db
3788	14	204	146.8	D
3852	15	12	155.5	D#/Eb
3916	15	76	164.8	E
3980	15	140	174.6	F
4044	15	204	185	F#/Gb
4108	16	12	196	G
4172	16	76	207.6	G#/Ab
4236	16	140	220	A
4300	16	204	233.1	A#/Bb
4364	17	12	246.9	B
4428	17	76	261.6	C
4492	17	140	277.2	C#/Db
4556	17	204	293.6	D
4620	18	12	311.1	D#/Eb
4684	18	76	329.6	E
4748	18	140	349.2	F
4812	18	204	370	F#/Gb
4876	19	12	392	G
4940	19	76	415.3	G#/Ab
5004	19	140	440	A
5068	19	204	466.2	A#/Bb
5132	20	12	493.9	B
5196	20	76	523.3	C
5260	20	140	554.4	C#/Db
5324	20	204	587.3	D
5388	21	12	622.3	D#/Eb
5452	21	76	659.3	E
5516	21	140	698.5	F
5580	21	204	740	F#/Gb
5644	22	12	784	G
5708	22	76	830.7	G#/Ab
5772	22	140	880	A
5836	22	204	932.4	A#/Bb
5900	23	12	987.8	B
5964	23	76	1046.6	C
6028	23	140	1108.8	C#/Db
6092	23	204	1174.7	D
6156	24	12	1244.6	D#/Eb
6220	24	76	1318.6	E
6284	24	140	1397	F
6348	24	204	1480.1	F#/Gb

TABLE A (continued)

Atari Tone	MSB	LSB	FREQ	NOTE
6412	25	12	1568.1	G
6476	25	76	1661.4	G#/Ab
6540	25	140	1760.1	A
6604	25	204	1864.8	A#/Bb
6668	26	12	1975.7	B
6732	26	76	2093.2	C
6796	26	140	2217.7	C#/Db
6860	26	204	2349.5	D
6924	27	12	2489.2	D#/Eb
6988	27	76	2637.3	E
7052	27	140	2794.1	F
7116	27	204	2960.2	F#/Gb
7180	28	12	3136.3	G
7244	28	76	3322.7	G#/Ab
7308	28	140	3520.3	A
7372	28	204	3729.7	A#/Bb
7436	29	12	3951.4	B
7500	29	76	4186.4	C
7564	29	140	4435.4	C#/Db
7628	29	204	4699.1	D
7692	30	12	4978.5	D#/Eb
7756	30	76	5274.6	E
7820	30	140	5588.2	F
7884	30	204	5920.5	F#/Gb
7948	31	12	6272.6	G
8012	31	76	6645.5	G#/Ab
8076	31	140	7040.7	A
8140	31	204	7459.4	A#/Bb

TABLE B

Atari Tone	MSB	LSB	FREQ
4941	19	77	415.7
4942	19	78	416
4943	19	79	416.4
4944	19	80	416.8
4945	19	81	417.2
4946	19	82	417.5
4947	19	83	417.9
4948	19	84	418.3
4949	19	85	418.7
4950	19	86	419.1
4951	19	87	419.4
4952	19	88	419.8
4953	19	89	420.2
4954	19	90	420.6
4955	19	91	421
4956	19	92	421.3
4957	19	93	421.7
4958	19	94	422.1
4959	19	95	422.5
4960	19	96	422.9
4961	19	97	423.2
4962	19	98	423.6
4963	19	99	424
4964	19	100	424.4
4965	19	101	424.8
4966	19	102	425.2
4967	19	103	425.5
4968	19	104	425.9
4969	19	105	426.3
4970	19	106	426.7
4971	19	107	427.1
4972	19	108	427.5
4973	19	109	427.8
4974	19	110	428.2
4975	19	111	428.6
4976	19	112	429
4977	19	113	429.4
4978	19	114	429.8
4979	19	115	430.2
4980	19	116	430.6
4981	19	117	431
4982	19	118	431.3
4983	19	119	431.7
4984	19	120	432.1
4985	19	121	432.5
4986	19	122	432.9
4987	19	123	433.3
4988	19	124	433.7
4989	19	125	434.1
4990	19	126	434.5
4991	19	127	434.9
4992	19	128	435.3
4993	19	129	435.6

Range: 2 semitones
Resolution: 1 Atari Tone (1/64 st)
Centered around A (440 Hz)

TABLE B (continued)

Atari Tone	MSB	LSB	FREQ
4994	19	130	436
4995	19	131	436.4
4996	19	132	436.8
4997	19	133	437.2
4998	19	134	437.6
4999	19	135	438
5000	19	136	438.4
5001	19	137	438.8
5002	19	138	439.2
5003	19	139	439.6
5004	19	140	440
5005	19	141	440.4
5006	19	142	440.8
5007	19	143	441.2
5008	19	144	441.6
5009	19	145	442
5010	19	146	442.4
5011	19	147	442.8
5012	19	148	443.2
5013	19	149	443.6
5014	19	150	444
5015	19	151	444.4
5016	19	152	444.8
5017	19	153	445.2
5018	19	154	445.6
5019	19	155	446
5020	19	156	446.4
5021	19	157	446.8
5022	19	158	447.2
5023	19	159	447.6
5024	19	160	448
5025	19	161	448.4
5026	19	162	448.8
5027	19	163	449.2
5028	19	164	449.6
5029	19	165	450
5030	19	166	450.4
5031	19	167	450.8
5032	19	168	451.3
5033	19	169	451.7
5034	19	170	452.1
5035	19	171	452.5
5036	19	172	452.9
5037	19	173	453.3
5038	19	174	453.7
5039	19	175	454.1
5040	19	176	454.5
5041	19	177	454.9
5042	19	178	455.3
5043	19	179	455.8

TABLE B (continued)

Atari Tone	MSB	LSB	FREQ
5044	19	180	456.2
5045	19	181	456.6
5046	19	182	457
5047	19	183	457.4
5048	19	184	457.8
5049	19	185	458.2
5050	19	186	458.6
5051	19	187	459.1
5052	19	188	459.5
5053	19	189	459.9
5054	19	190	460.3
5055	19	191	460.7
5056	19	192	461.1
5057	19	193	461.6
5058	19	194	462
5059	19	195	462.4
5060	19	196	462.8
5061	19	197	463.2
5062	19	198	463.6
5063	19	199	464.1
5064	19	200	464.5
5065	19	201	464.9
5066	19	202	465.3
5067	19	203	465.7

TABLE C

+ SLOPE	- SLOPE	SEMI/SEC	DB/SEC	M	E
0	128	0	0	0	0
1	159	0.11	1.9	1	0
2	158	0.23	3.81	2	0
3	157	0.35	5.72	3	0
4	156	0.47	7.62	4	0
5	155	0.59	9.53	5	0
6	154	0.71	11.44	6	0
7	153	0.83	13.35	7	0
8	152	0.95	15.25	8	0
9	151	1.07	17.16	9	0
10	150	1.19	19.07	10	0
11	149	1.31	20.98	11	0
12	148	1.43	22.88	12	0
13	147	1.54	24.79	13	0
14	146	1.66	26.7	14	0
15	145	1.78	28.61	15	0
16	144	1.9	30.51	16	0
17	143	2.02	32.42	17	0
18	142	2.14	34.33	18	0
19	141	2.26	36.23	19	0
20	140	2.38	38.14	20	0
21	139	2.5	40.05	21	0
22	138	2.62	41.96	22	0
23	137	2.74	43.86	23	0
24	136	2.86	45.77	24	0
25	135	2.98	47.68	25	0
26	134	3.09	49.59	26	0
27	133	3.21	51.49	27	0
28	132	3.33	53.4	28	0
29	131	3.45	55.31	29	0
30	130	3.57	57.22	30	0
31	129	3.69	59.12	31	0
32	160	0	0	0	1
33	191	0.47	7.62	1	1
34	190	0.95	15.25	2	1
35	189	1.43	22.88	3	1
36	188	1.9	30.51	4	1
37	187	2.38	38.14	5	1
38	186	2.86	45.77	6	1
39	185	3.33	53.4	7	1
40	184	3.81	61.03	8	1
41	183	4.29	68.66	9	1
42	182	4.76	76.29	10	1
43	181	5.24	83.92	11	1
44	180	5.72	91.55	12	1
45	179	6.19	99.18	13	1
46	178	6.67	106.81	14	1
47	177	7.15	114.44	15	1
48	176	7.62	122.07	16	1

TABLE C (continued)

+ SLOPE	- SLOPE	SEMI/SEC	DB/SEC	M	E
49	175	8.1	129.69	17	1
50	174	8.58	137.32	18	1
51	173	9.05	144.95	19	1
52	172	9.53	152.58	20	1
53	171	10.01	160.21	21	1
54	170	10.49	167.84	22	1
55	169	10.96	175.47	23	1
56	168	11.44	183.1	24	1
57	167	11.92	190.73	25	1
58	166	12.39	198.36	26	1
59	165	12.87	205.99	27	1
60	164	13.35	213.62	28	1
61	163	13.82	221.25	29	1
62	162	14.3	228.88	30	1
63	161	14.78	236.51	31	1
64	192	0	0	0	2
65	223	1.9	30.51	1	2
66	222	3.81	61.03	2	2
67	221	5.72	91.55	3	2
68	220	7.62	122.07	4	2
69	219	9.53	152.58	5	2
70	218	11.44	183.1	6	2
71	217	13.35	213.62	7	2
72	216	15.25	244.14	8	2
73	215	17.16	274.65	9	2
74	214	19.07	305.17	10	2
75	213	20.98	335.69	11	2
76	212	22.88	366.21	12	2
77	211	24.79	396.72	13	2
78	210	26.7	427.24	14	2
79	209	28.61	457.76	15	2
80	208	30.51	488.28	16	2
81	207	32.42	518.79	17	2
82	206	34.33	549.31	18	2
83	205	36.23	579.83	19	2
84	204	38.14	610.35	20	2
85	203	40.05	640.86	21	2
86	202	41.96	671.38	22	2
87	201	43.86	701.9	23	2
88	200	45.77	732.42	24	2
89	199	47.68	762.93	25	2
90	198	49.59	793.45	26	2
91	197	51.49	823.97	27	2
92	196	53.4	854.49	28	2
93	195	55.31	885	29	2
94	194	57.22	915.52	30	2
95	193	59.12	946.04	31	2

TABLE C (continued)

+ SLOPE	- SLOPE	SEMI/SEC	DB/SEC	M	E
96	224	0	0	0	3
97	255	7.62	122.07	1	3
98	254	15.25	244.14	2	3
99	253	22.88	366.21	3	3
100	252	30.51	488.28	4	3
101	251	38.14	610.35	5	3
102	250	45.77	732.42	6	3
103	249	53.4	854.49	7	3
104	248	61.03	976.56	8	3
105	247	68.66	1098.63	9	3
106	246	76.29	1220.7	10	3
107	245	83.92	1342.77	11	3
108	244	91.55	1464.84	12	3
109	243	99.18	1586.91	13	3
110	242	106.81	1708.98	14	3
111	241	114.44	1831.05	15	3
112	240	122.07	1953.12	16	3
113	239	129.69	2075.19	17	3
114	238	137.32	2197.26	18	3
115	237	144.95	2319.33	19	3
116	236	152.58	2441.4	20	3
117	235	160.21	2563.47	21	3
118	234	167.84	2685.54	22	3
119	233	175.47	2807.61	23	3
120	232	183.1	2929.68	24	3
121	231	190.73	3051.75	25	3
122	230	198.36	3173.82	26	3
123	229	205.99	3295.89	27	3
124	228	213.62	3417.96	28	3
125	227	221.25	3540.03	29	3
126	226	228.88	3662.1	30	3
127	225	236.51	3784.17	31	3