



| REV | REVISIONS DESCRIPTION | DATE | APPROVED |
|-----|----------------------------|---------|----------|
| 3 | ENGR REL PER ERC E0340 : | 3/20/84 | HW |
| 4 | INCORPORATED PER ERC E0481 | 3/6/84 | JR |

ENGINEERING RELEASED

| | | | | |
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| | | D. Albrecht | 3/1/84 | |
| NEXT ASSY | USED ON | CHECKED | DATE | TITLE GATE ARRAY "BARBARA" |
| | | F. Hooper | 3/20/84 | |
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| | | APPROVED J. Weber 4/2/84 | SCALE | SHEET 1 OF 14 |

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1.0 SCOPE

This document is a preliminary specification of the electrical and mechanical requirements for a 40 pin custom high speed CMOS gate array I.C. device designated for use on the "TONG" project. The device is currently under development and there may be revisions to this document before it is Production Released.

2.0 APPLICABLE DOCUMENTS

The following documents, at the revision which is in effect on the date of the Purchase Order, shall form part of this specification to the extent referenced herein.

- a. CO99901 - Qualification and Reliability Requirements for Integrated Circuits and Discrete Semiconductors.
- b. CO99902 - Handling of Devices Susceptible to Static Discharge.
- c. CO99905 - External Visual and Solderability Requirements.
- d. CO99906 - Internal Visual Requirements for Atari Semiconductors.
- e. CO21538 - Electrostatic Discharge Sensitivity Testing.
- f. CO99931 - Dual In-Line Package, General Specifications.

3.0 DEVIATIONS

Product sold to Atari, Inc. under this specification must be identical to original approved samples. Any changes to the product must receive Atari, Inc. sample reapproval prior to delivery. Any deviation from this specification, or from any of the above listed applicable documents, must be approved in writing through the current Atari Deviation Procedure prior to any deviation taking place.



4.0 PRECEDENCE

This specification, including all approved deviations, shall be the governing document for device acceptance. In the event of conflict between this document and any other document, contract, specification or requirement, the manufacturer is responsible to notify Atari, Inc. for written disposition from the affected functional group(s), as identified within this document.

5.0 GENERAL REQUIREMENTS

5.1 ELECTROSTATIC DISCHARGE

Parts must conform to the requirements of the Atari, Inc. Specification #CO21538, Electrostatic Discharge Sensitivity Testing.

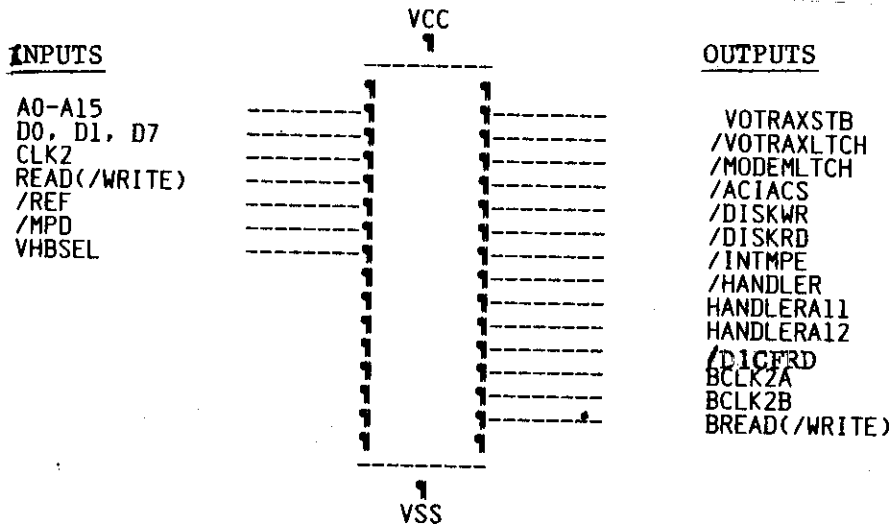
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5.2 MARKING

Minimally, parts must be marked permanently and legibly as per Atari, Inc. Specification #C099901 para. 10.1.12 with:

- a. Atari Part Number
- b. Date Code
- c. Copyright Symbol and information:
 - © ATARI (Year); year must be represented as either the full year (e.g. 1983) or the last two digits (e.g. 83)
- d. Vendor or industry recognized identification symbol
- e. Pin #1 Identification

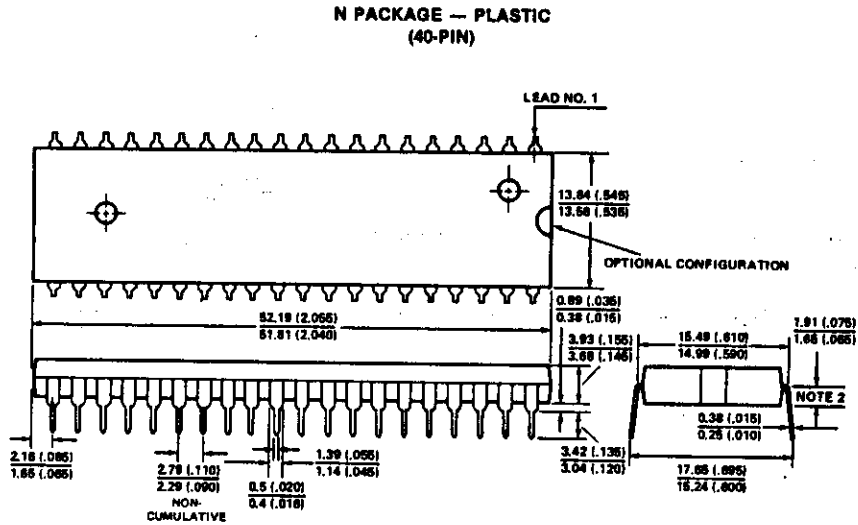
5.3 BLOCK DIAGRAM



Note: See Section 13.6 for pin assignment.

5.4 PACKAGE DESCRIPTION

Package shall be void-free plastic.



5.5 LEAD INTEGRITY AND SOLDERABILITY

As per Atari, Inc. Specification #C099901, para. 10.1.11 Lead Integrity and 10.1.16 Solderability.

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6.0 ABSOLUTE MAXIMUM RATINGS

Limits beyond which the life of the part may be impaired. It is NOT implied that the device should be operated at these limits. If the part is operated at or near these limits, applicable manufacturers' derating calculations must be imposed.

| ITEM | CHARACTERISTIC | LIMITS | UNITS |
|------|---|--------------|------------------|
| 6.1 | SUPPLY VOLTAGE V_{cc} TO GND (V_{cc}) | -0.5 TO +7.0 | V |
| 6.2 | VOLTAGE APPLIED TO ANY INPUT (V_{ai}) | -0.5 TO +7.0 | V |
| 6.3 | VOLTAGE APPLIED TO ANY OUTPUT (V_{ao}) | -0.5 TO +7.0 | V |
| 6.4 | POWER DISSIPATION (P_d) | 75.0 | mW |
| 6.5 | JUNCTION TEMP. $T_a=70^\circ$ (T_j) | TBD | $^\circ\text{C}$ |
| 6.6 | OPERATING TEMPERATURE (T_a) | 0 TO 70 | $^\circ\text{C}$ |
| 6.7 | STORAGE TEMPERATURE (T_{stj}) | -55 TO +150 | $^\circ\text{C}$ |



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7.0 STATIC CHARACTERISTICS

Unless otherwise specified:

- a. $0 \leq T_a \leq 70^\circ\text{C}$
- b. $4.75 \leq V_{cc} \leq 5.25$
- c. Positive current flows into the device
- d. $C_{LOAD} = 50\text{pF}$

| ITEM | CHARACTERISTICS | CONDITION | LIMITS | | UNITS |
|------|---|--|--------|-----|-------|
| | | | min | max | |
| 7.1 | INPUT VOLTAGE HIGH (VIH) | | 2.0 | Vcc | V |
| 7.2 | INPUT VOLTAGE LOW (VIL) | | -0.3 | 0.8 | V |
| 7.3 | INPUT CURRENT (I _I) | $0 \leq V_{in} \leq 5.25$ Vcc = 5.25 | -10 | 10 | uA |
| 7.4 | OUTPUT VOLTAGE HIGH (VOH) | Vcc = 4.75 I _{OH} = -100uA | 2.4 | 5.0 | V |
| 7.5 | OUTPUT VOLTAGE LOW (VOL) | Vcc = 4.75 I _{OL} = 1.6 mA | 0 | 0.4 | V |
| 7.6 | OUTPUT LEAKAGE CURRENT HIGH (I _{LOH}) | HIGH Z OUTPUT V _O = 5.0 Vcc = 5.25 | -1.0 | 1.0 | uA |
| 7.7 | OUTPUT LEAKAGE CURRENT LOW (I _{LOL}) | HIGH Z OUTPUT V _O = 0.0 Vcc = 5.25 | -1.0 | 1.0 | uA |
| 7.8 | POWER SUPPLY CURRENT (I _{CC}) | Vcc = 5.25V ALL INPUTS = Vcc DEVICE IS ACTIVE | TBD | 14 | mA |
| 7.9 | BREAKDOWN VOLTAGE (Bv) | I _{in} =10uA, ALL OTHER=0V; TEST ALL INPUTS ONE AT A TIME | 7 | | V |



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8.0 DYNAMIC CHARACTERISTICS

Unless otherwise specified:



- a. $0^{\circ} \leq T_a \leq 70^{\circ}\text{C}$.
- b. $4.75 \leq V_{cc} \leq 5.25$
- c. All waveforms and dynamic parameters tested at 1 std TTL load/50pF.
- d. Ref. dynamic test set up section 10.0
- e. Ref. timing diagrams section 9.2

| ITEM | PARAMETER | SYMBOL | MIN | MAX | UNIT |
|------|---|-----------------------|-----|----------|----------|
| 8.1 | Input to Output Prop. Delay Except Bread, BCLK 2 A/B | t_{PHL} , t_{PHL} | | 35 15 | ns ns |
| 8.2 | Clock to Output Prop. Delay | t_{PHL} , t_{PHL} | | 25 | ns |
| 8.3 | Setup Time Data to Clock | t_s | 5 | | ns |
| 8.4 | Hold Time Data to Clock | t_h | 5 | | ns |
| 8.5 | Clock Pulse Width | t_w | 50 | | ns |

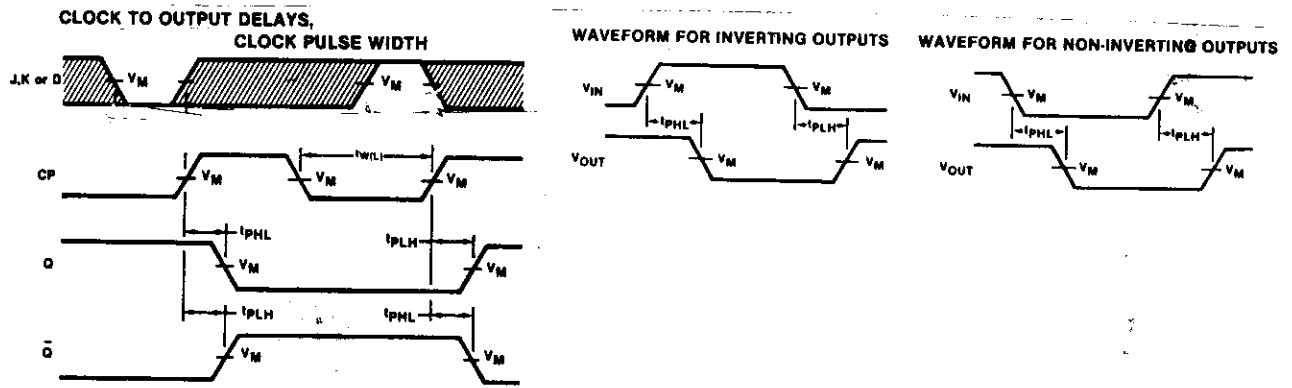
9.0 DYNAMIC TEST WAVEFORMS

9.1 TIMING DEFINITIONS

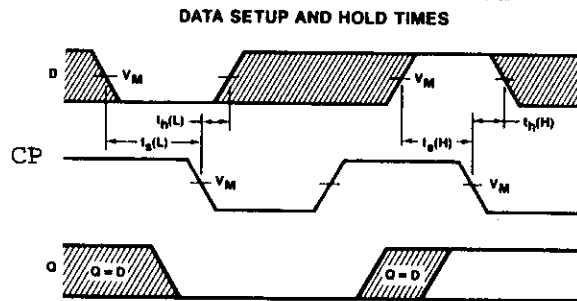
- a. Rise and Fall times are measured at 10 to 90% of the waveform maximum amplitude.
- b. Applied waveform specifications:
 $t_r = t_f \leq 9\text{ns} \pm 10\%$

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9.2 TIMING DIAGRAMS



Where: $V_M = 1.5V$
 t_s = setup time
 t_h = hold time
 t_{PHL} = prop. delay high to low
 t_{PLH} = prop. delay low to high



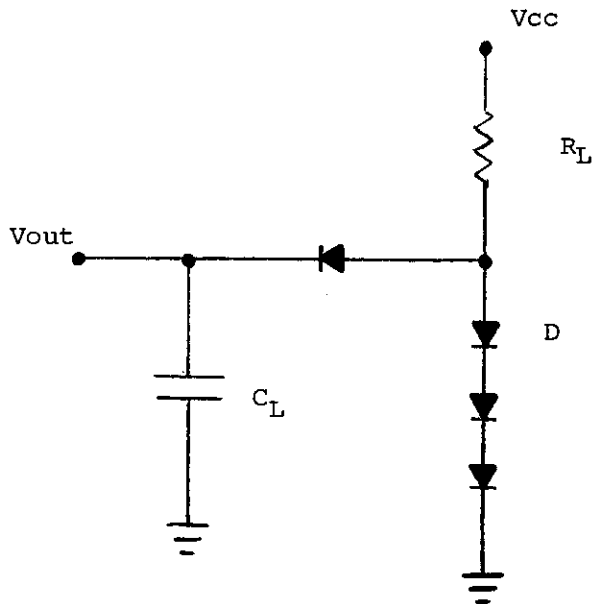
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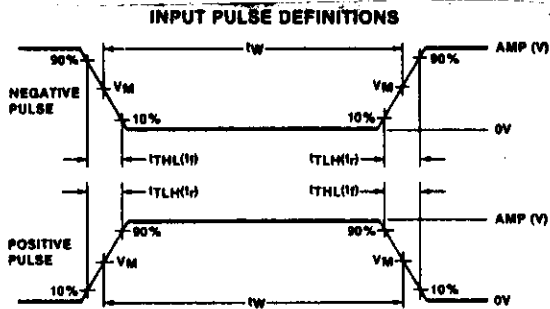
10.0 DYNAMIC TEST SET-UP

10.1 LOAD CIRCUIT FOR OUTPUT PINS (or equiv. 1 std. TTL load/50pF)



Where: $C_L = 50\text{pF}$
 $R_L = 2\text{K}$
 $D = 1\text{N}916, 1\text{N}3064$ or equivalent

10.2 Input Pulse Definitions



Where: $V_m = 1.5\text{V}$
 Amplitude = 3.0V
 $t_w = 50\text{ns}$
 Repetition rate = 10mhz

11.0 LOGIC EQUATIONS

 GATE ARRAY "A" 40 PIN PLASTIC ("BARBARA")

INPUT DEFINITIONS: ("/" DENOTES ACTIVE LOW INPUT)

***** ALL INPUTS ARE DEFINED AS SEEN AT THE INPUT PAD *****

INPUT WITH "*" DENOTES DC LEVEL SIGNALS, WHICH ARE SET DURING PREVIOUS CYCLE.

| | | |
|------------------------|---|----------------------|
| | +5V | VCC, POWER SUPPLY |
| | GND | VSS |
| | A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15 | CPU ADDRESS BUS |
| | D0, D1, D7 | CPU DATA BUS 0, 1, 7 |
| * | VHBSSEL | VHANDLER BANK SELECT |
| | CLK2 | CPU PHASE 2 CLOCK |
| | READ(/WRITE) | CPU READ(/WRITE) |
| | /REF | CPU /REFRESH |
| * | /MPD | /MATH PAK DISABLE |
| TOTAL INPUT PIN COUNT: | | *** 26 *** |

INTERNAL REGISTER (D TYPE "74LS74" FLIPFLOP) SIGNAL DEFINITIONS:

***** DATA IS CLOCKED AT THE TRAILING EDGE (HIGH TO LOW) OF THE CLOCK *****

CLOCK SIGNAL FOR ALL THREE FLIPFLOPS:

CLK= A15*A14*/A13*A12*/A11*/A10*/A9*A8*A7* A6*A5*A4*A3*A2*A1*A0*/READ*/REF*/CLK2 DIFFH WRITE.

DS0(OUTPUT)= D0 CLOCKED BY CLK

DS1(OUTPUT)= D1 CLOCKED BY CLK

DS7(OUTPUT)= D7 CLOCKED BY CLK



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OUTPUT DEFINITIONS: ("/" DENOTES ACTIVE LOW OUTPUT)

***** ALL OUTPUTS ARE DEFINED AS SEEN AT THE OUTPUT PAD *****
 ***** ACTIVE LOW OUTPUTS ARE INVERTED BEFORE GOING TO PAD *****

VOTRAXSTB= A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7* (ACTIVE HIGH)
 /A6*/A5*/A4*/A3*/A2*/REF*CLK2 D100H-D103H (R/W)
 +A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7*
 /A6*/A5*/A4*/A3*A2*/A1*/REF*CLK2 D104H-D105H (R/W)

/VOTRAXLTCH= A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7*
 /A6*/A5*/A4*/A3*A2*A1*/REF*CLK2 D106H-D107H (R/W)

/MODEMLTCH= A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7*
 /A6*/A5*/A4*A3*/A2*/READ*/REF*CLK2 D108H-D10BH (W)

/ACIACS= A15*A14*/A13*A12*/A11*/A10*/A9*A8*
 /A7*/A6*/A5*/A4*A3*A2*/REF D10CH-D10FH (R/W)

/DISKWR= A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7*
 /A6*/A5*A4*/A3*/A2*/READ*/REF*DS0*CLK2 D110H-D113H (W)

/DISKRD= A15*A14*/A13*A12*/A11*/A10*/A9*A8*/A7*
 /A6*/A5*A4*/A3*A2*READ*/REF*DS0*CLK2 D114H-D117H (R)

/INTMPE= DSO PBI DEVICE 0
 +DS1 PBI DEVICE 1
 +DS7 PBI DEVICE 7
 +MPD /MATH PAK DISABLE INV.

/HANDLER= A15*A14*/A13*A12*A11*/REF*DS0 PBI DEVICE 0, 1 AND 7
 +A15*A14*/A13*A12*A11*/REF*DS1 AT D800H-DFFFH, OVER
 +A15*A14*/A13*A12*A11*/REF*DS7 LAPPING OS-MATHPAK.

HANDLERA11= /DS7*DS1 PBI DEVICE 1 and 7
 +VHBSSEL* DS7

HANDLERA12= DS7 PBI DEVICE 7 * /VHBSSEL or
 PBI DEVICE 7 * VHBSSEL

/D1CFRD A15*A14*/A13*A12*/A11*/A10*/A9*A8*A7 D1CFH READ
 A6*A5*A4*A3*A2*A1*A0*READ*/REF*CLK2

BREAD(/WRITE)= READ(/WRITE) BUFFERED READ(/WRITE)

BCLK2A CLK2 BUFFERED CLK2

BCLK2B CLK2 BUFFERED CLK2

TOTAL OUTPUT PIN COUNT: *** 14 ***

TOTAL PIN COUNT: *** 40 ***

HANDLER A11 AND A12 DECODING TABLE:

| VHBSSEL | DS7 | DS1 | DS0 | HA12 | HA11 |
|---------|-----|-----|-----|------|------|
| x | 0 | 0 | 1 | 0 | 0 |
| x | 0 | 1 | x | 0 | 1 |
| 0 | 1 | x | x | 1 | 0 |
| 1 | 1 | x | x | 1 | 1 |



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12.0 ELECTRICAL CHARACTERIZATION TESTING

Characterization and device performance tests are to be done on a Sentry 7 with high voltage test heads.

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13.0 PIN ASSIGNMENT

| <u>Pin #</u> | <u>Signal</u> |
|--------------|---------------|
| 1 | /DISKWR |
| 2 | /DISKRD |
| 3 | /D1CFRD |
| 4 | /HANDLER |
| 5 | DS0 |
| 6 | DS1 |
| 7 | DS7 |
| 8 | MPD |
| 9 | INTMPE |
| 10 | VHBSEL |
| 11 | HANDLERA11 |
| 12 | HANDLERA12 |
| 13 | BREAD |
| 14 | READ |
| 15 | VCC |
| 16 | VSS |
| 17 | /ACIACS |
| 18 | /MODEMLTCH |
| 19 | /VOTRAXLTCH |
| 20 | VOTRAXSTB |
| 21 | A15 |
| 22 | A14 |
| 23 | A13 |
| 24 | A12 |
| 25 | A11 |
| 26 | A10 |
| 27 | A9 |
| 28 | A8 |
| 29 | A7 |
| 30 | A6 |
| 31 | A5 |
| 32 | A4 |
| 33 | A3 |
| 34 | A2 |
| 35 | A1 |
| 36 | A0 |
| 37 | /REF |
| 38 | CLK2 |
| 39 | BCLK2A |
| 40 | BCLK2B |



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